

Hall B RICH DAQ

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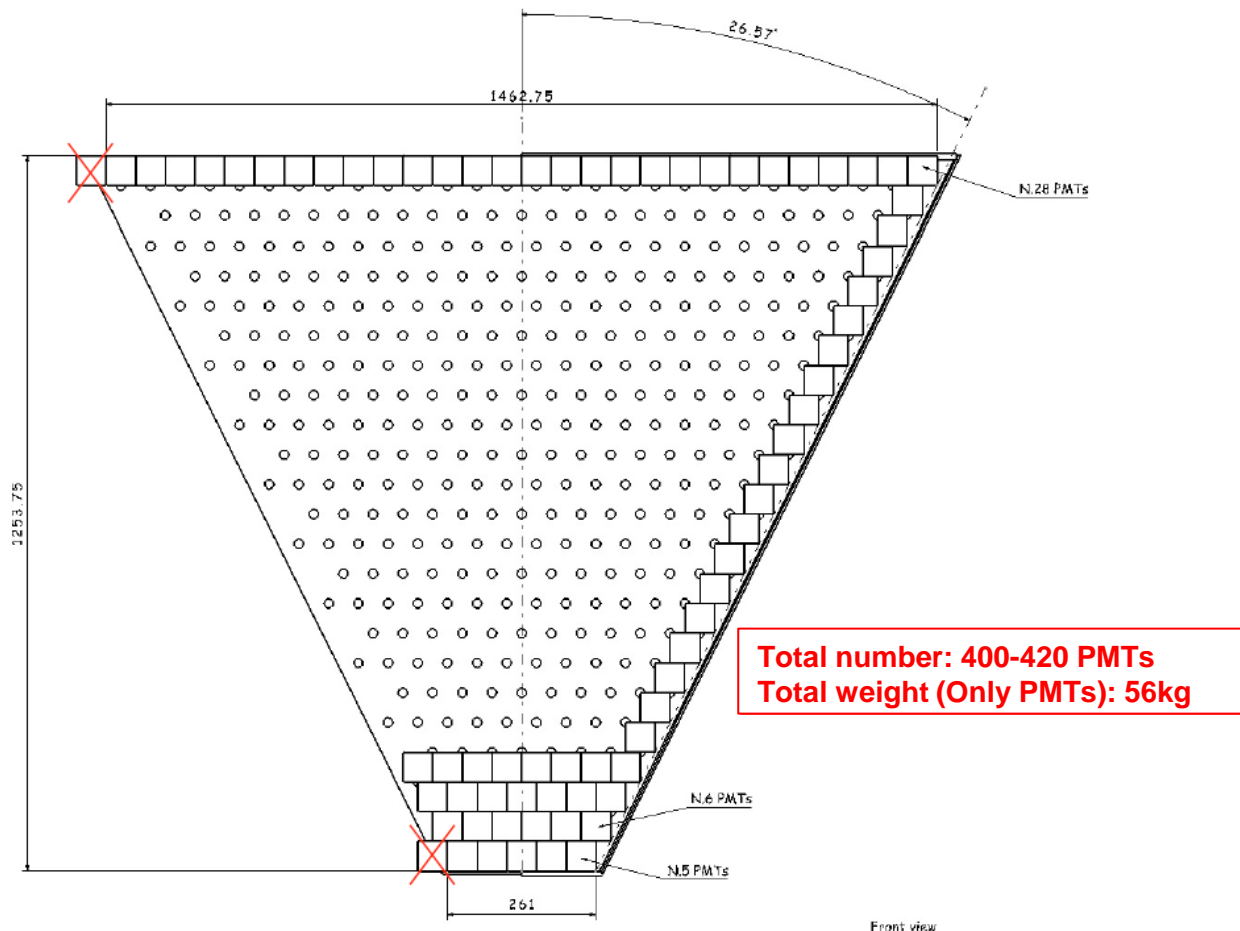
Overview

1. RICH Detector PMT Array
2. PMT Motherboard Assemblies
3. MAROC3 FPGA Board
4. DREAM FPGA Board
5. Power/Signal Cabling
6. Backend DAQ

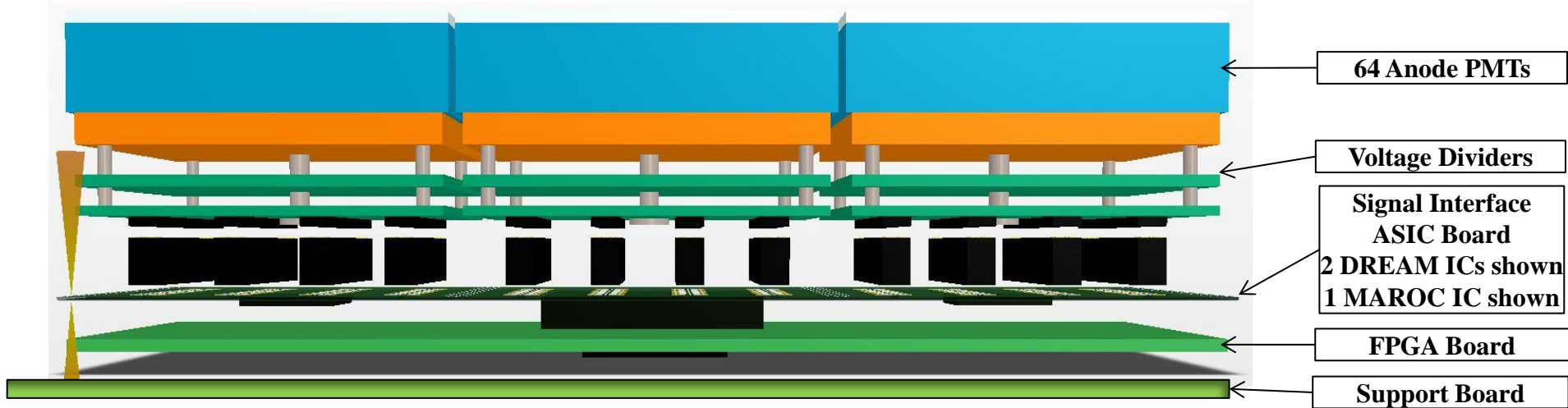
RICH PMT Array

~400 Multi-Channel PMTs for single RICH sector

- ~25,000 PMT channels
- Need high voltage. low voltage. slow control. digitization & readout



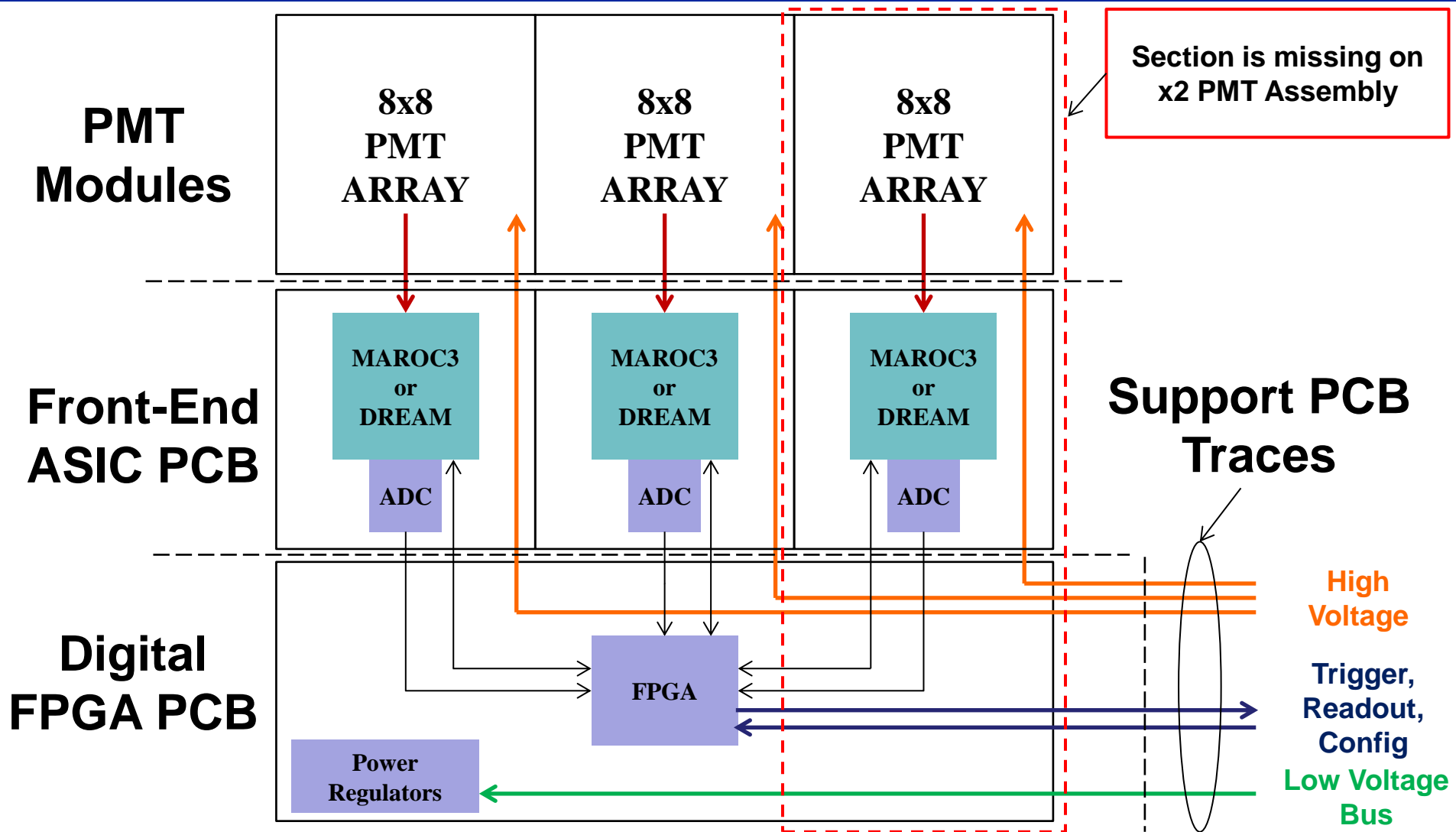
PMT Assembly



Mosaic Idea: group PMTs to reduce digital electronics resources

- Design two motherboards
 - x3 PMT Motherboard
 - x2 PMT Motherboard
- One FPGA for each Motherboard supports I/O for ASIC chips
- Reduction of cabling
- Another board would support x2/x3 PMT assemblies
 - Provides mechanical support
 - Low voltage distribution
 - High voltage distribution (option)

PMT Assembly



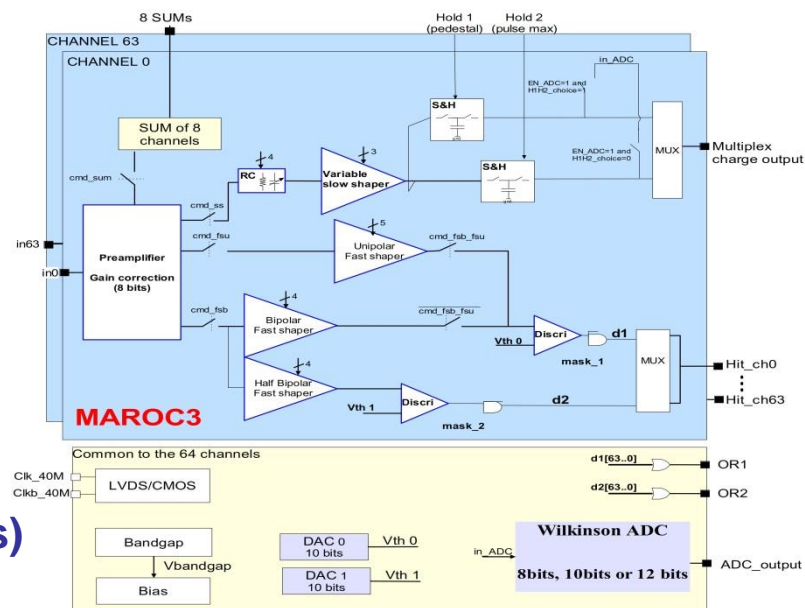
Digital FPGA PCB – MAROC3

MAROC3 Signals

- MAROC3 provides 64 digital outputs
- MAROC3 provides 1 muxed analog output
- Slow controls

MAROC3 FPGA Board Processing

- ~1ns TDC on 192 channels (3 chips * 64 signals)
- Buffer data for 8us (trigger decision time)
- Trigger will extract 1ns timing resolution hits to build event
- 3 ADC analog channels (3 chips * 1 analog mux output)
- Flash ADC, buffer data for 8us (trigger decision time)
- Trigger will extract pulse data to build event (for calibration/testing)
- 2.5Gbps SerDes provides reference clock, trigger, & readout data

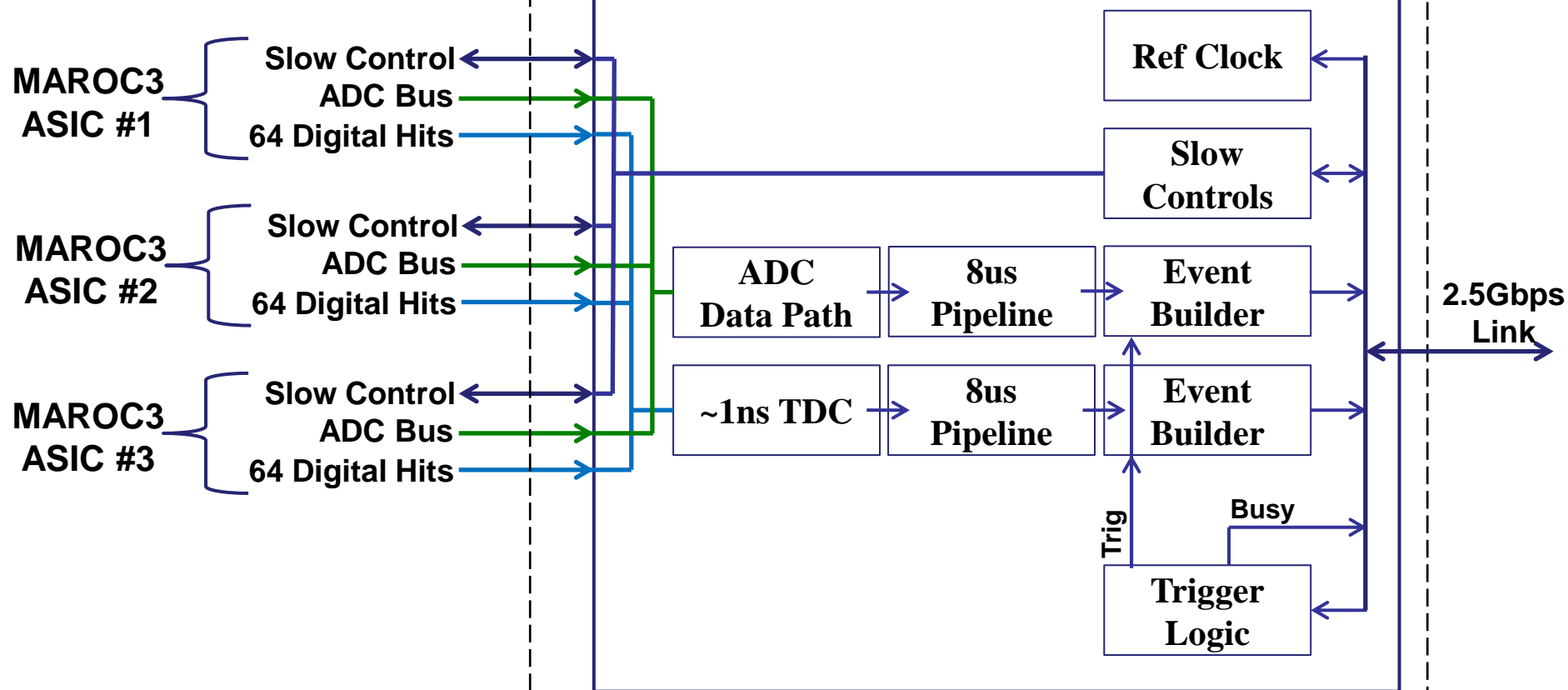


Digital FPGA PCB – MAROC3 continued...

Front-End ASIC PCB

Digital FPGA PCB

Support PCB



Digital FPGA PCB – DREAM

DREAM Signals

- **DREAM provides 1 analog output**
- **Digital hit OR**
- **Slow controls**

DREAM FPGA Board Processing

- 20MHz Flash ADC converter on readout
- DREAM buffers data for 8us (trigger decision time)
- Trigger will force ADC conversion on section of trigger window for all channels
- Trigger can sample 1 to a few points per channel/trigger
- Event builder can interpolate multiple samples to enhance timing resolution
- Event builder can provide integral of pulse
- FPGA will zero suppress channels and build event from channels over threshold
- 2.5Gbps SerDes provides reference clock, trigger, & readout data

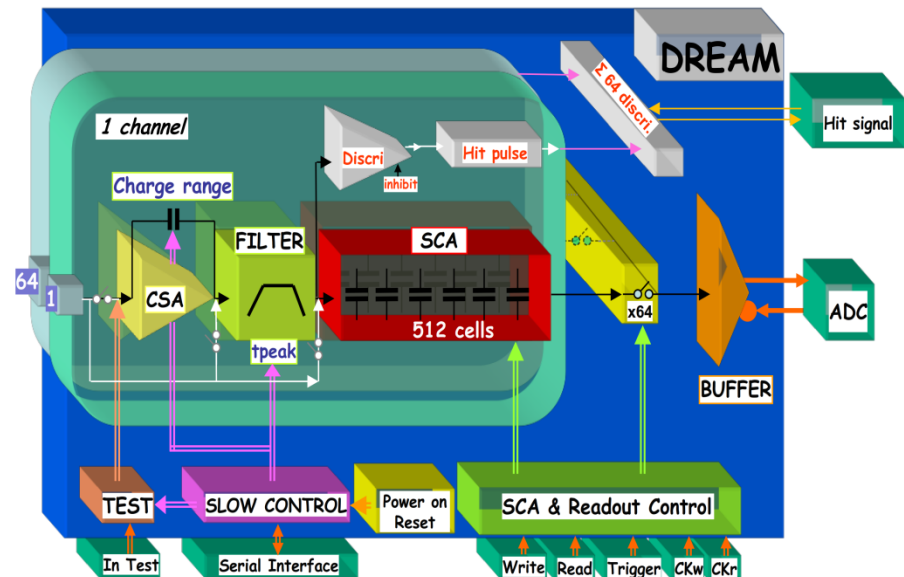


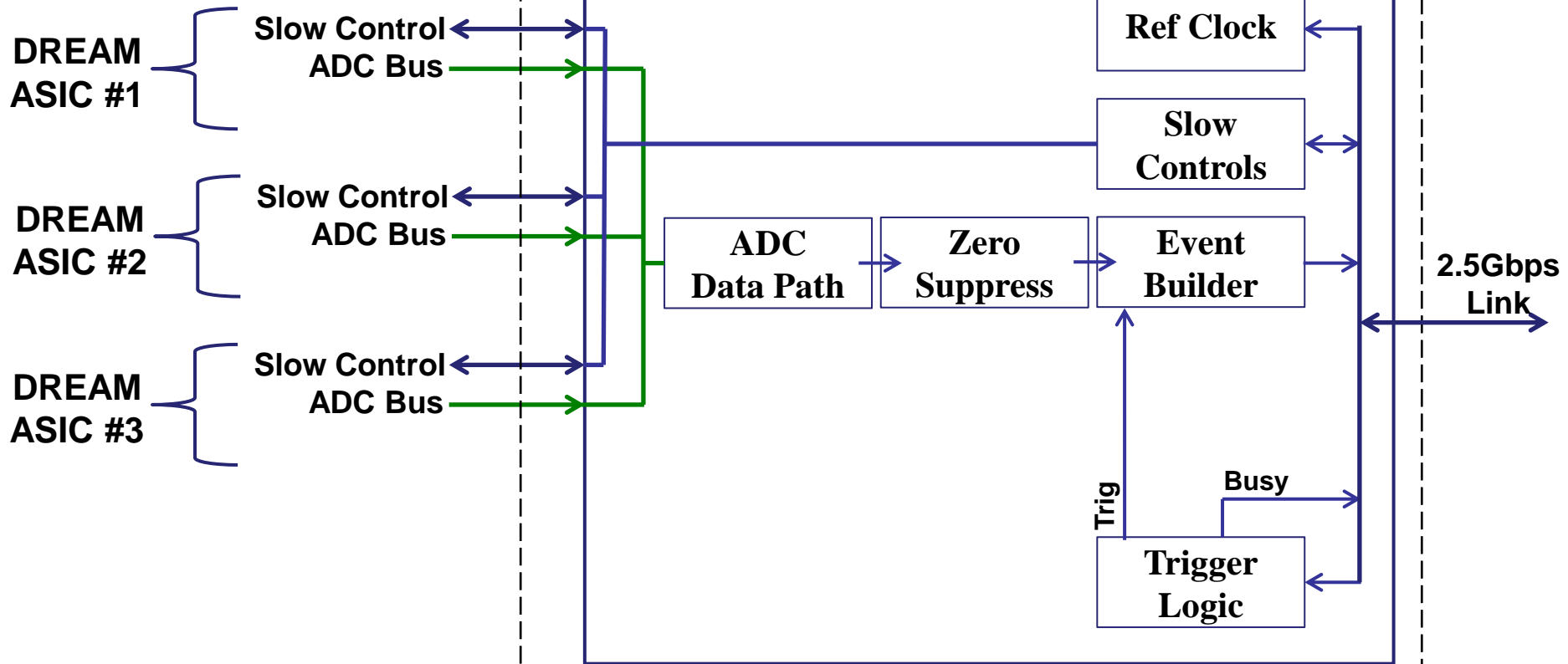
Fig. 1: Block diagram of the DREAM chip.

Digital FPGA PCB – DREAM continued...

Front-End ASIC PCB

Digital FPGA PCB

Support PCB



Trigger/Readout/Config

Serial Link to each x2/x3 PMT motherboard

- Full duplex running @ 2.5Gbps
- Fixed latency link (in DAQ -> PMT direction)
- Connected to backend DAQ VME system

Function in DAQ -> PMT direction:

- Synchronous reference clock @ PMT motherboard (<1ns uncertainty)
- Fixed latency trigger signal @ PMT motherboard
- Slow control writes

Function in PMT -> DAQ direction:

- Slow control read
- Trigger event readout

Support PCB

Support PCB for Mosaic PMT Assemblies

- Split-up backplane:**

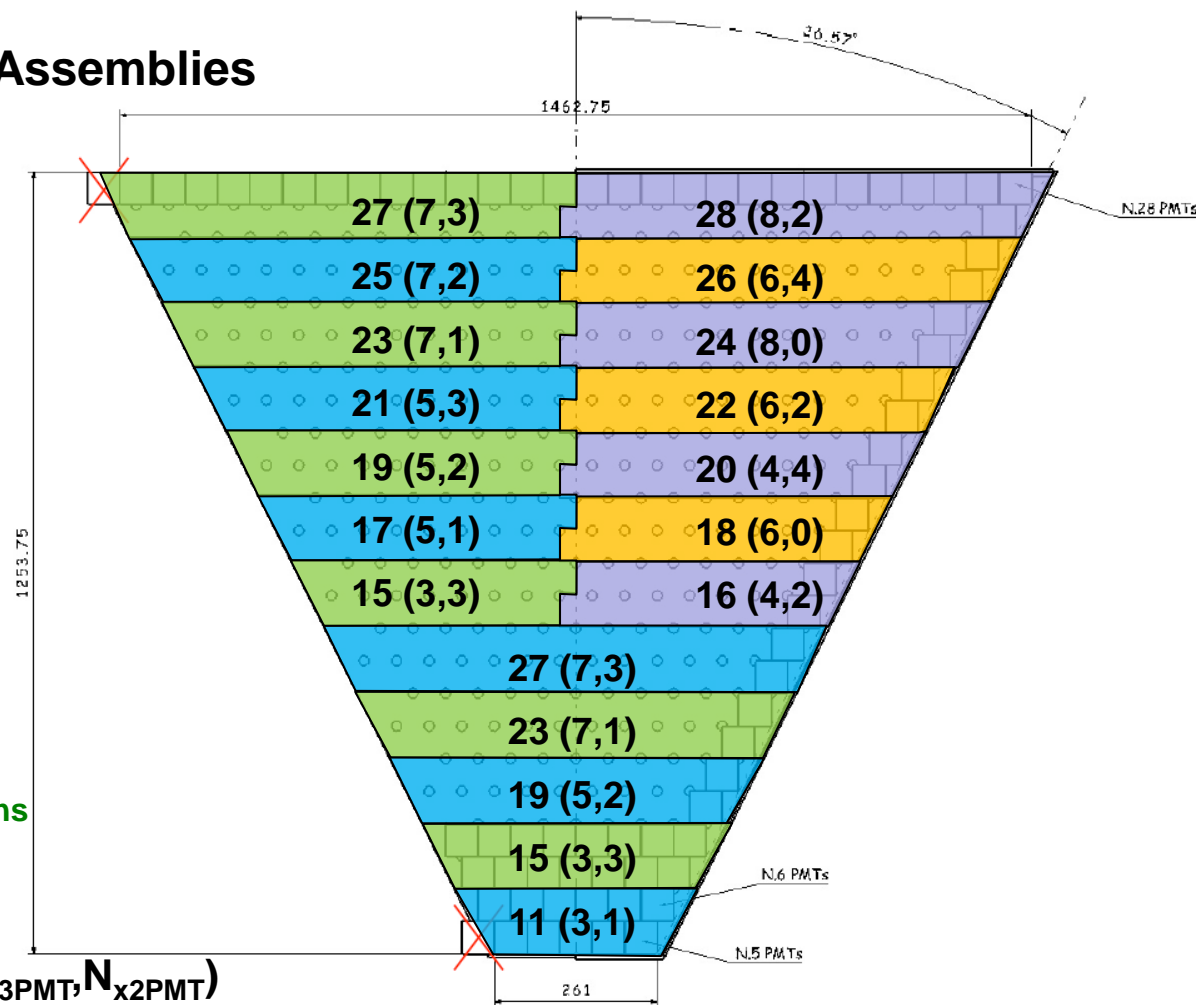
- Break into smaller pieces for easier manufacturing

- Keep it simple:**

- No active components
- Traces + connectors only
- Thick (~6mm) 4-6 Layer PCB
- Shielded high voltage traces
- Impedance controlled DAQ bus

- Board Counts**

- QTY 106: PMT Assembly x3 Style
- QTY 39: PMT Assembly x2 Style
- QTY 19: Unique Support PCB sections



*Numbers in the array: N_{PMT} (N_{x3PMT}, N_{x2PMT})

N_{PMT} = Number of PMT in region

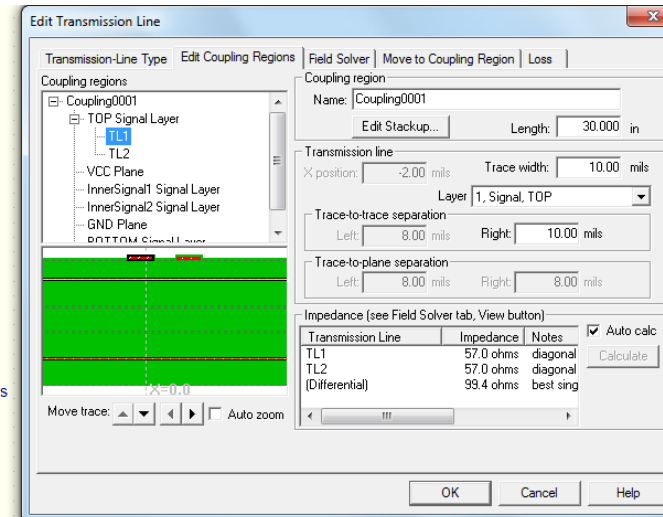
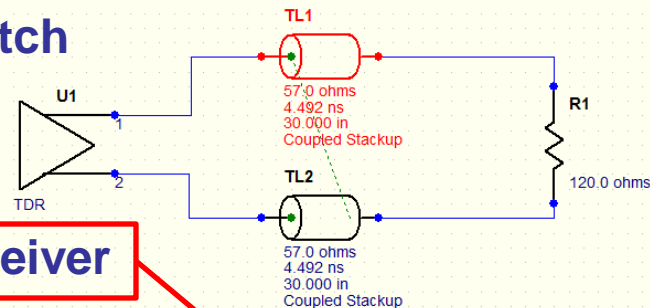
N_{x3PMT} = Number of x3 style PMT Motherboards

N_{x2PMT} = Number of x2 style PMT Motherboards

Gigabit Line Driver over Support PCB

2.5Gbps loss simulation over 30" of FR4 PCB Substrate

- Low cost FR370 material
- Driver rise/fall times: 10ps
- 20% Termination Mismatch
- Differential line 100ohm
- No equalization used
- Wide eye opening at receiver



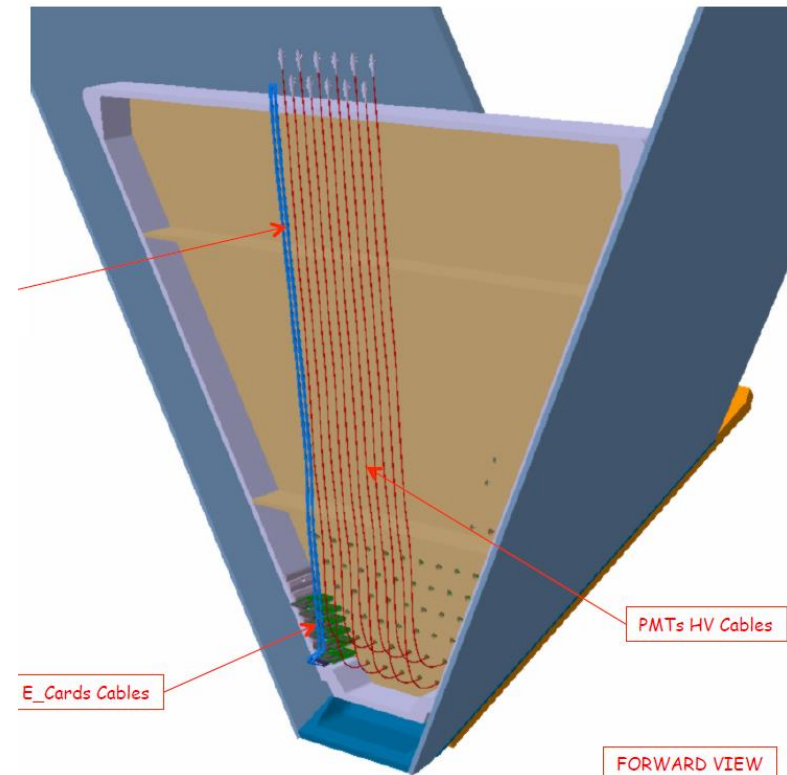
High Voltage

Option 1: Cable from PMT directly to HV supply

- Most flexible option

Option 2: Run PMT HV lines on Support PCB

- Use multi-channel HV bus connectors at Support PCB edges
- Probably only makes sense to do if HV channels are to be grouped together



Low Voltage

Low voltage is for:

- **Front-End PCB**
 - ~640mW for each DREAM ASIC, ~224mW for each MAROC3 ASIC
- **Digital FPGA PCB**
 - A few W for each x2/x3 PMT motherboard (QTY = ~145)
- **Optical Transceivers**
 - ~1W for roughly every 4 x2/x3 PMT motherboard (QTY ~42)

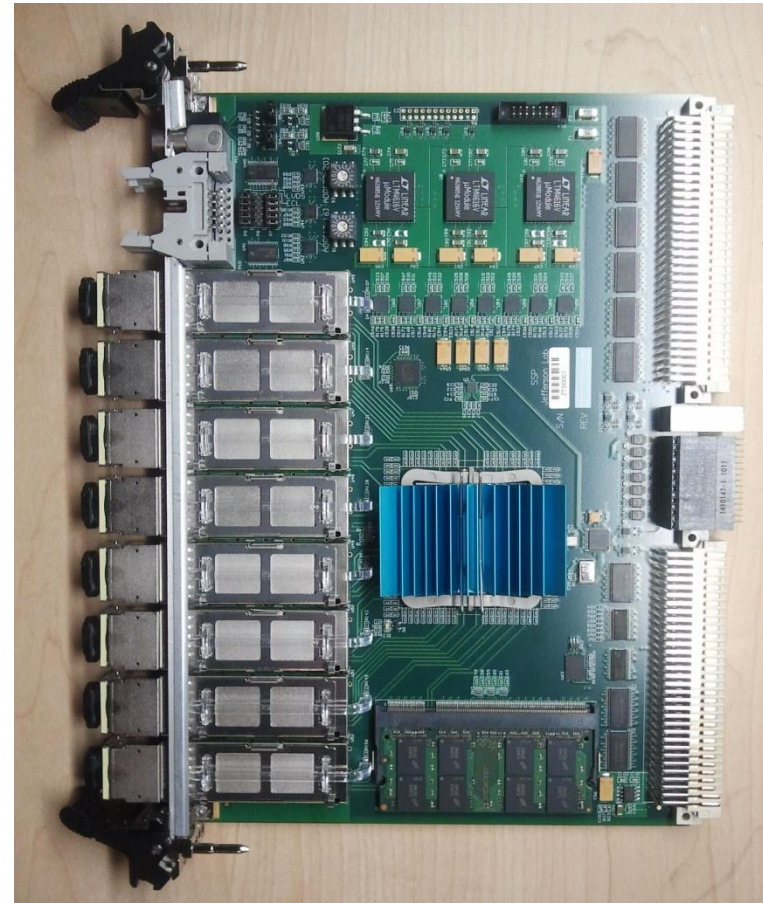
Bus low voltage on Support PCB

- Deliver low voltage cable to each support PCB section
- Likely in the range of 4 to 5V, regulated down locally on PMT motherboard

Backend DAQ

Use Jlab SSP (developed for GlueX and CLAS12):

- VME/VXS DAQ Optics FPGA Module
 - Slow control to each PMT FPGA
 - Readout bridge for PMT motherboards
 - Trigger signal to PMT motherboards
 - Reference clock to PMT motherboards
- Readout
 - VME 2eSST @ 200MB/s
 - Large event buffer (4GByte)
- Fiber Link
 - 32 Full-duplex links
 - >100 meter range
 - Up to 5Gbps per link



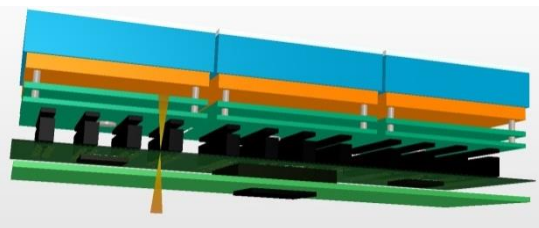
RICH DAQ Occupancies

CLAS12 running conditions: 20kHz trigger

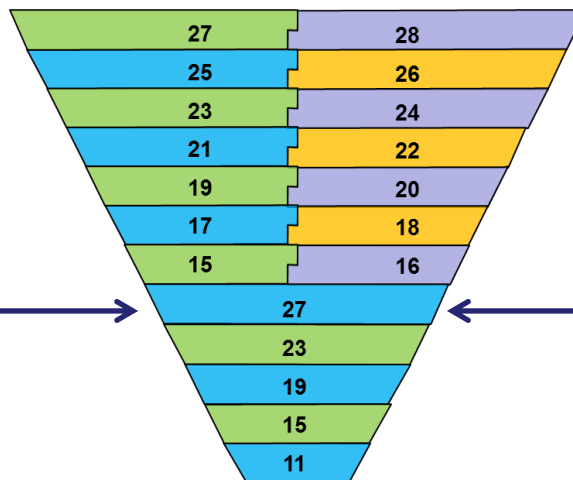
- VME Bus provides 200MB/s readout rate
- Readout controller with 10GBE
- RICH Sector: ~25,000 PMT Channels
- Occupancy Limit
 - MAROC3 hit: 32bit event word for each hit (1ns resolution time, channel ID)
 - 10bits: timestamp, 13bits: channel ID
 - DREAM hit: 32bit event word for each hit (1-20ns resolution time, channel ID, integral)
 - 10bits: timestamp, 13bits: channel ID, 9bits: charge estimate
 - $200\text{MB/s} / 20\text{kHz} / 32\text{bits} = 2\text{k Hits per event}$
 - $2\text{k} / 25\text{k} \Rightarrow$ maximum 8% sustained occupancy
- Limit could be improved by
 - Put SSP modules in multiple VME crates (2 crates gives 16% sustained occupancy)
 - Put VME bus readout limit to 320MB/s (gives ~12% sustained occupancy)

Full Readout Data Path

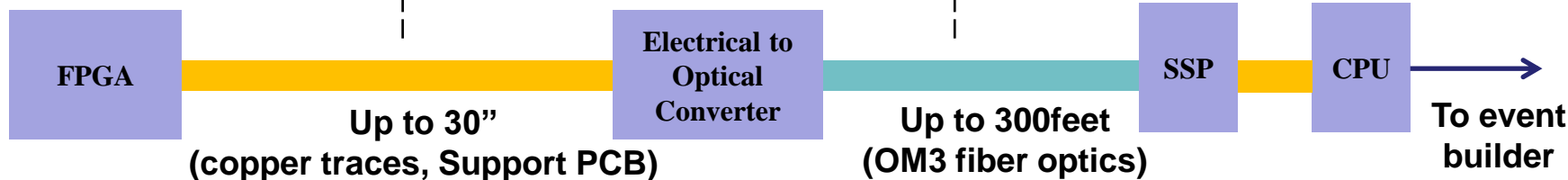
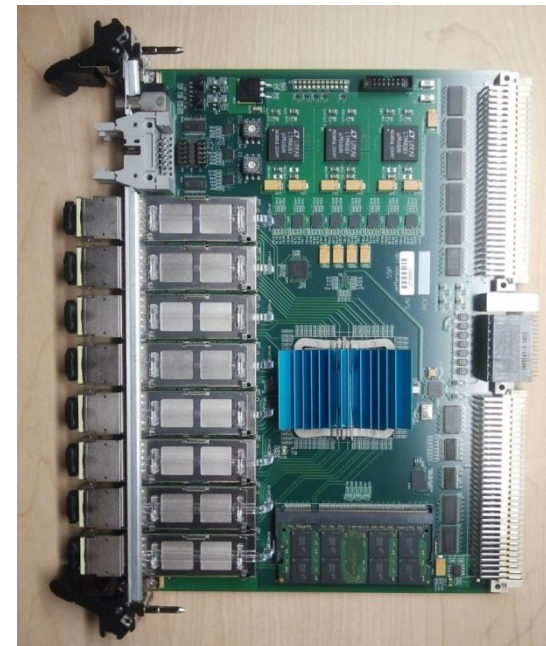
**PMT Motherboard
(QTY ~145)**



**Support PCB
(QTY ~19)**



**SSP (VME/VXS)
(QTY ~6)**



Details to work out/check...

1. Mechanical optimizations/mounting
2. Fixed latency gigabit link
3. Radiation tolerance for optics & ICs
4. Magnetic fields, thermal concerns

Summary

- **Modular design allows for a low risk (cost) prototype and easier maintenance**
- **Backend hardware already designed and compatible with CLAS12 DAQ**