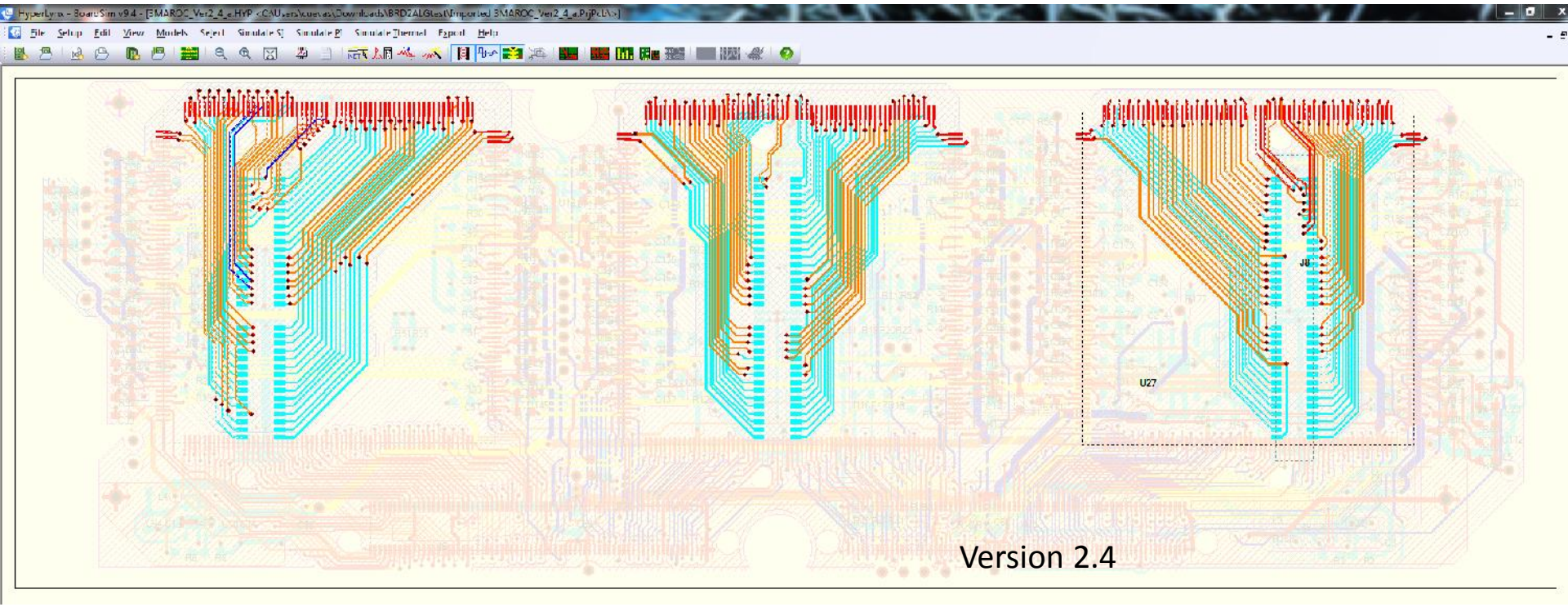
Hall B 12GeV RICH Detector

Electronics

ASIC circuit board layout notes
Version 2_4_a

C. Cuevas
2016 Sept 13



- Input signal traces occupy several layers – Good
- Length of input traces varies from 1.7” to 0.39” – OK, unavoidable given input connection orientation
- This layout version has careful consideration for input return path ‘plane’ (Analog GND)
- Careful consideration to separate digital lines from analog input layers
- Digital signal return plane is separate from analog signal return plane
- Digital signal routing has been changed to minimized cross over sections of input signal traces

Circuit Board Layer Stack

Stackup Editor

File Edit View Help

Basic | Dielectric | Metal | Z0 Planning | Manufacturing | Custom View

	Visible	Color	Pour Draw Style	Layer Name	Type	Usage	Thickness mils oz	Er	Test Width mils	Z0 ohm	Thermal Conductivity Btu/hrFF	Description
1	☑		Hatched	TOP	Metal	Signal	0.869	<Auto>	6.299	59.5	227.476	
2				DE_TOP	Dielectric	Substrate	8	4.5			0.173	
3	☑		Hatched	LAYER2	Metal	Signal	0.869	<Auto>	7.874	57.2	227.476	
4				DE_LAYER2	Dielectric	Substrate	8	4.5			0.173	
5	☑		Hatched	LAYER3	Metal	Plane	0.869	<Auto>	14.173	38.8	227.476	
6				DE_LAYER3	Dielectric	Substrate	8	4.5			0.173	
7	☑		Hatched	LAYER4	Metal	Plane	0.869	<Auto>	6.299	63.7	227.476	
8				DE_LAYER4	Dielectric	Substrate	8	4.5			0.173	
9	☑		Hatched	LAYER5	Metal	Signal	0.869	<Auto>	6.299	62.1	227.476	
10				DE_LAYER5	Dielectric	Substrate	8	4.5			0.173	
11	☑		Hatched	BOTTOM	Metal	Signal	0.869	<Auto>	6.299	59.5	227.476	

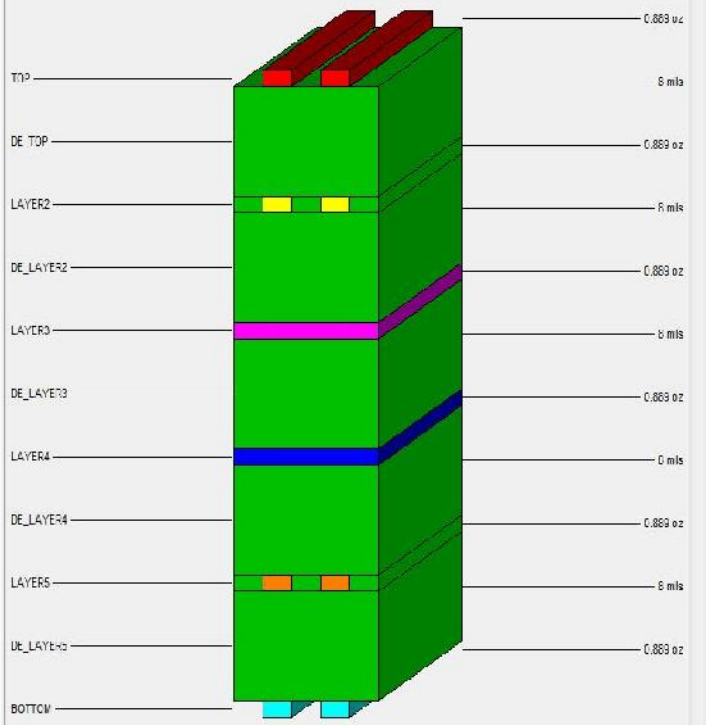
Measurement units: English

Meta thickness as: Weight

Zo for inner layers is not 50 Ohm
but layer stack may not be accurate.

Top and Bottom layer impedance
makes sense given no plane directly
Beneath traces. (Close to 100 Ohm)

Version 2_4_a



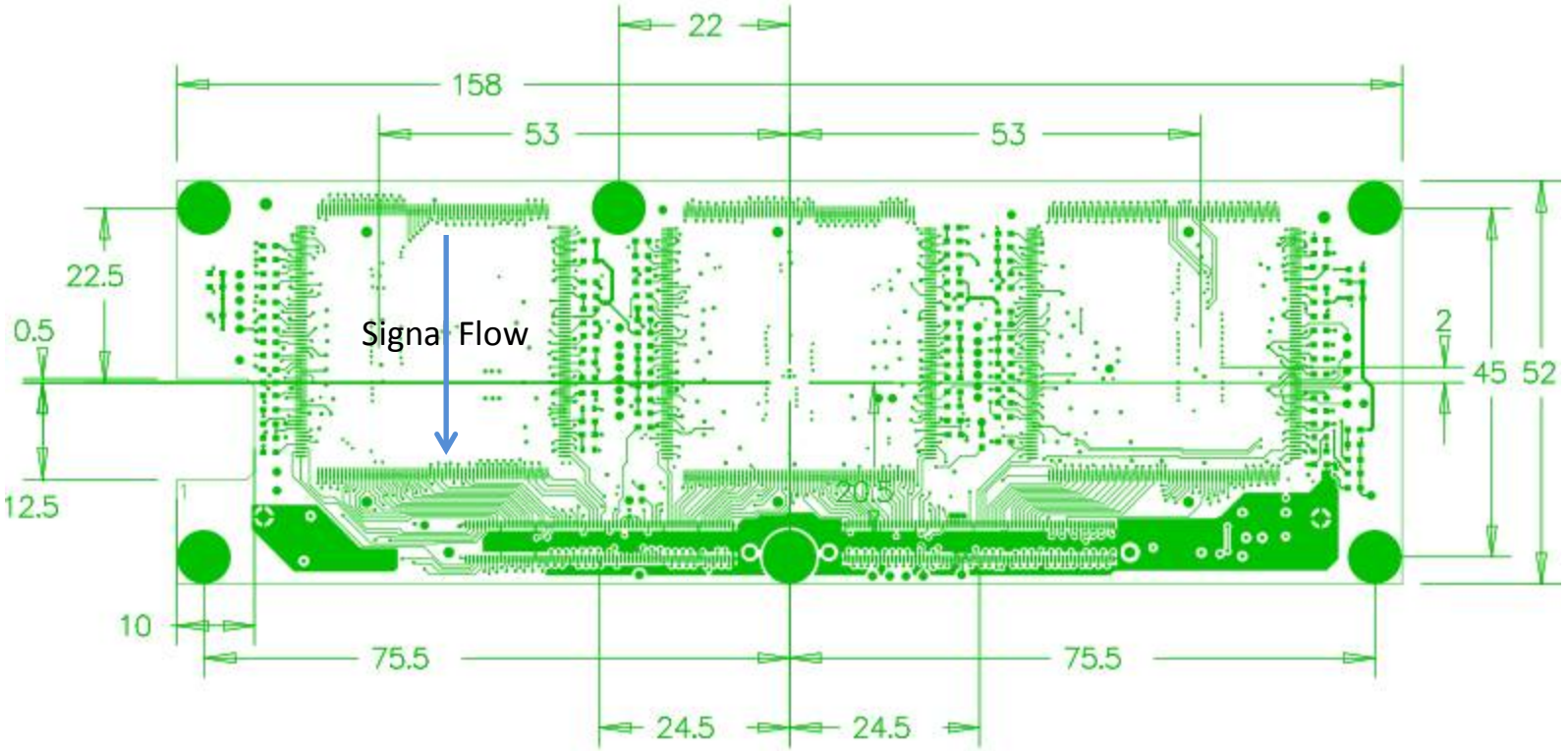
☑ Draw proportionally Total thickness: 47.2 mils

☑ Use layer colors

No errors found in stackup.

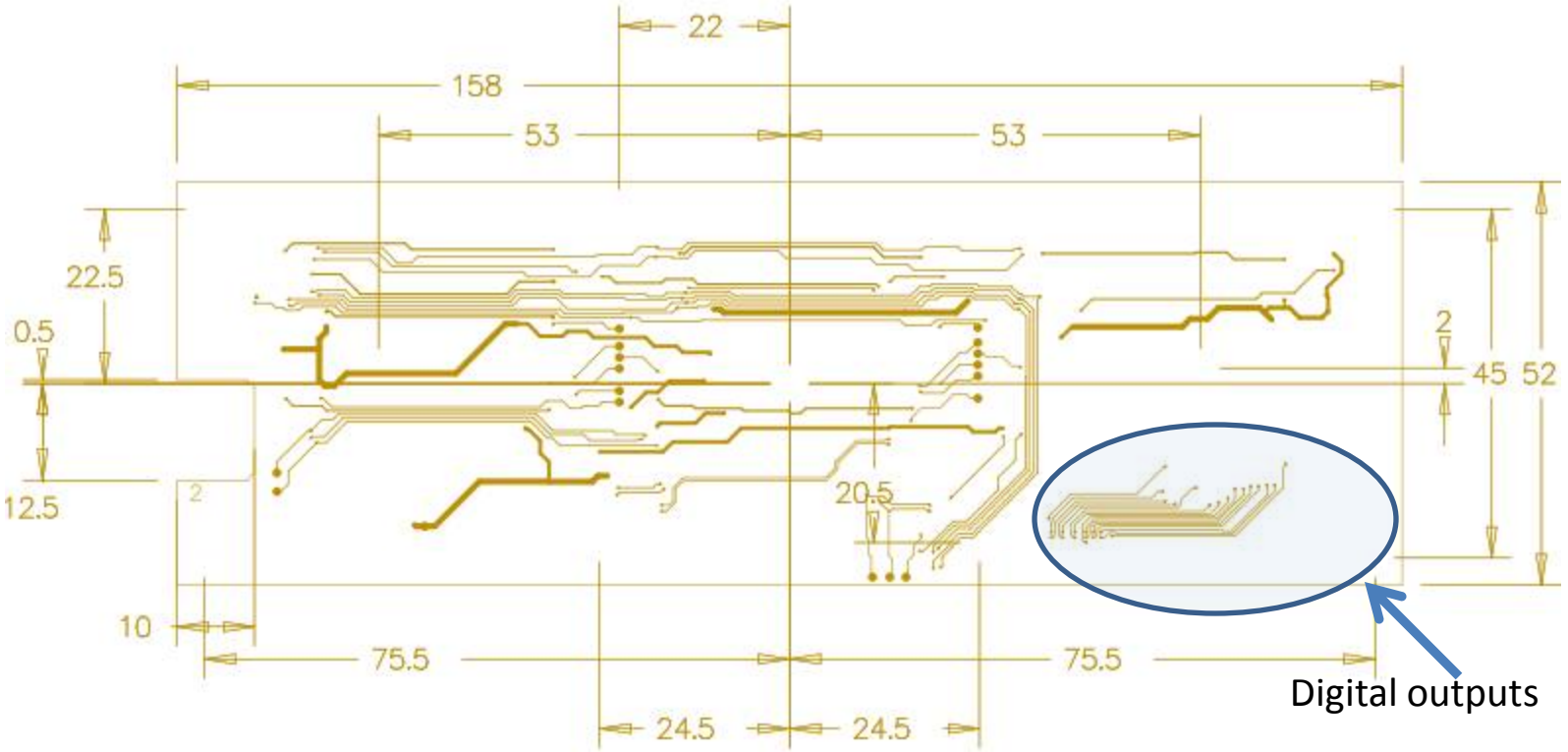
TOP

- MAROC3 chips have nice ‘flow through’ design
  - i.e. Inputs on one side; Outputs on other side
  - Digital control lines/power pins on the sides
  - Layout shows nice routing of digital outputs to FPGA connector



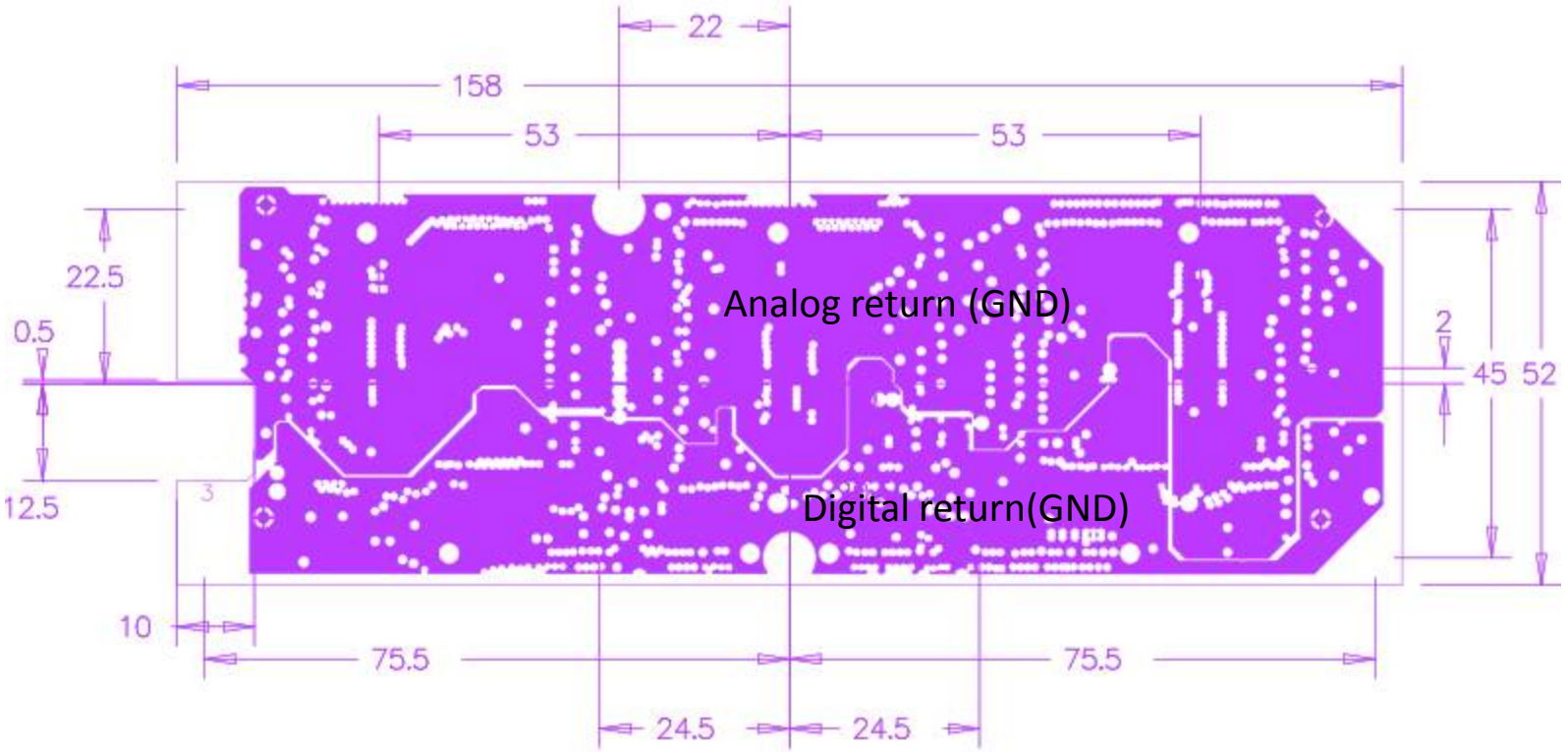
MID1

- Digital control lines on this layer with a few output traces
- Some traces are DC bias voltages (VDD)
- These traces are separated from analog input traces with plane layers beneath



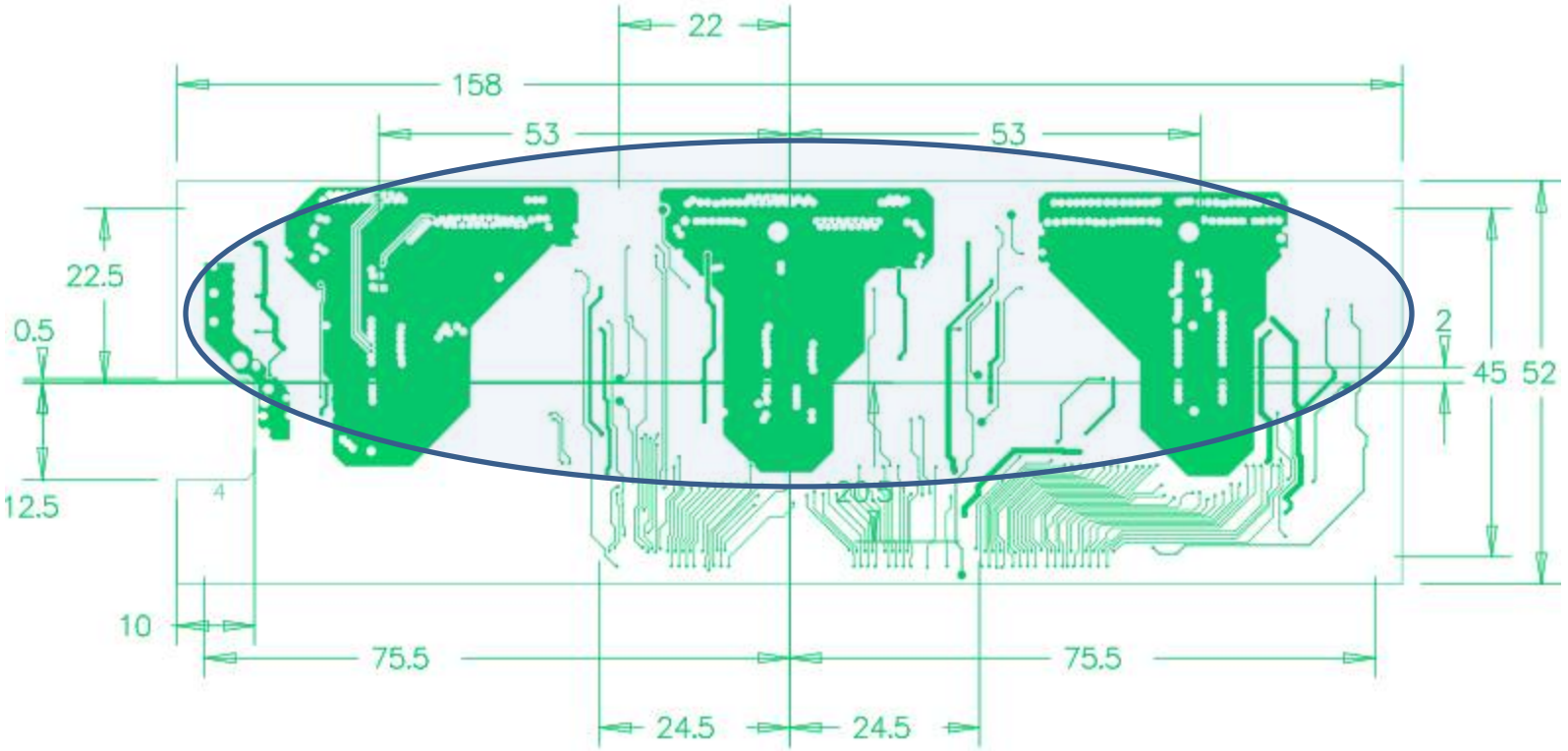
MID2

- Picture shows that this layer is effectively a GND plane
- Note that the plane is split
- Digital and Analog signal return paths are separated.

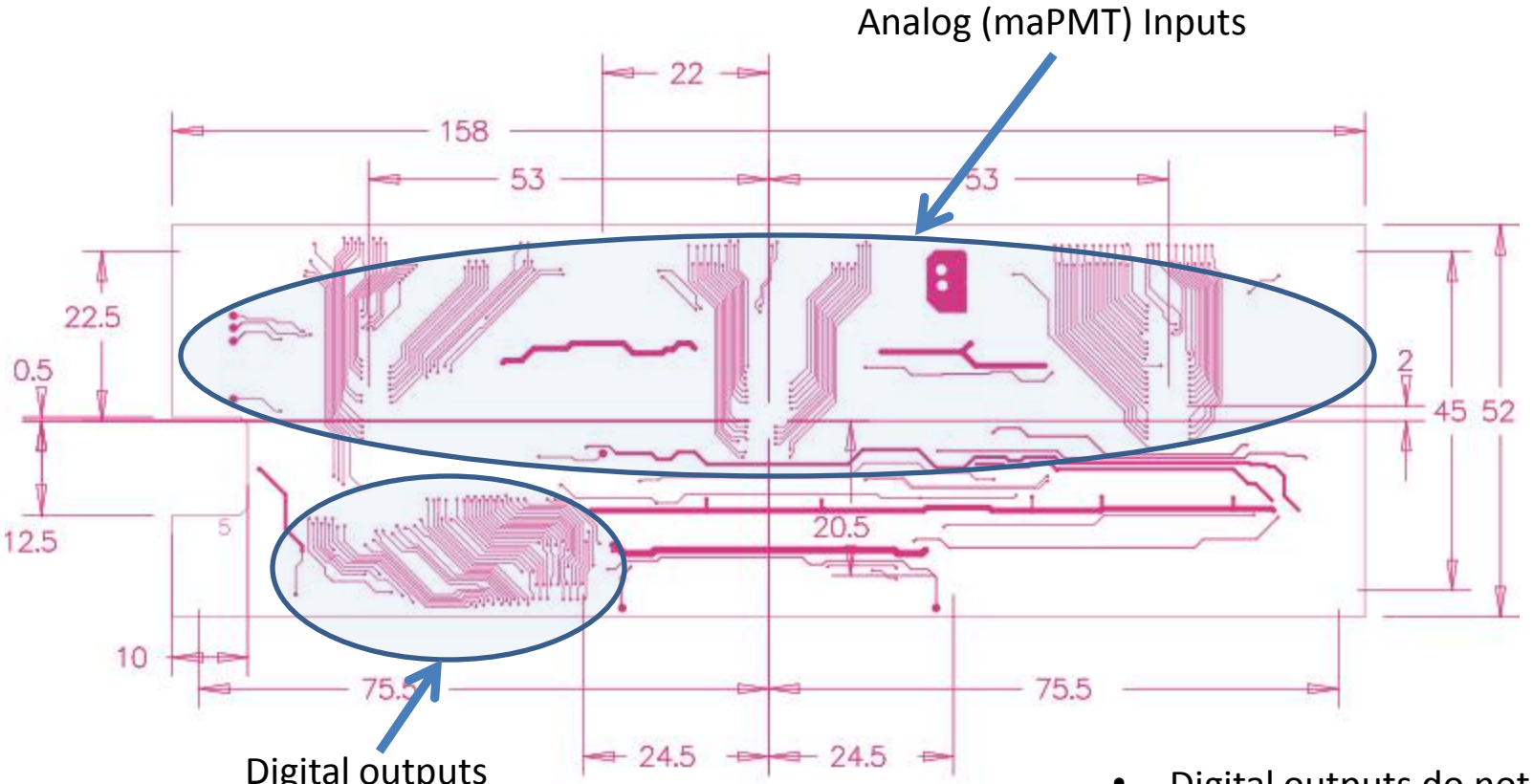


MID3

- Large copper polygons for Analog signal return path(GND)
- Digital signal traces exist but separated from Analog input trace routing areas.
- These return paths are a significant design improvement

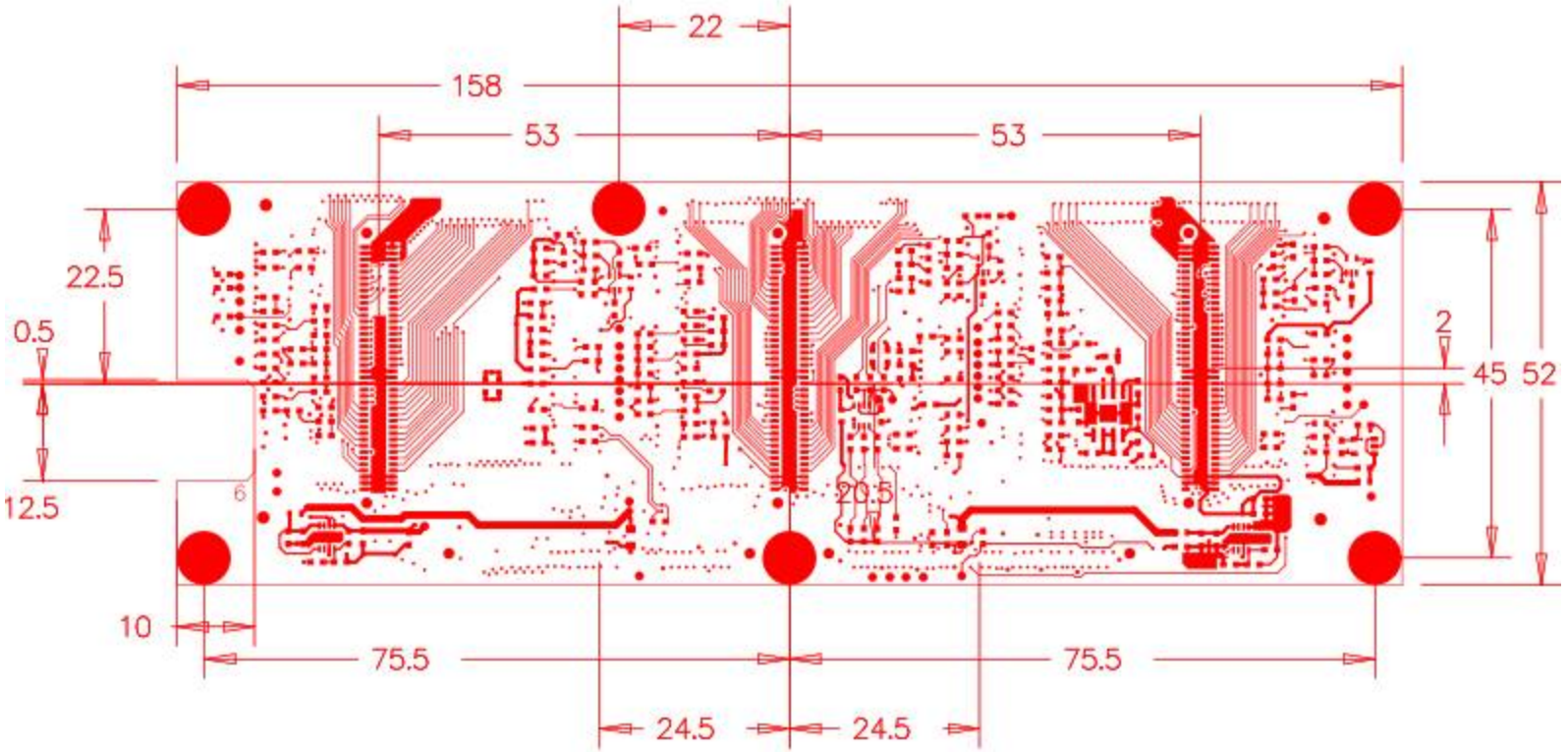


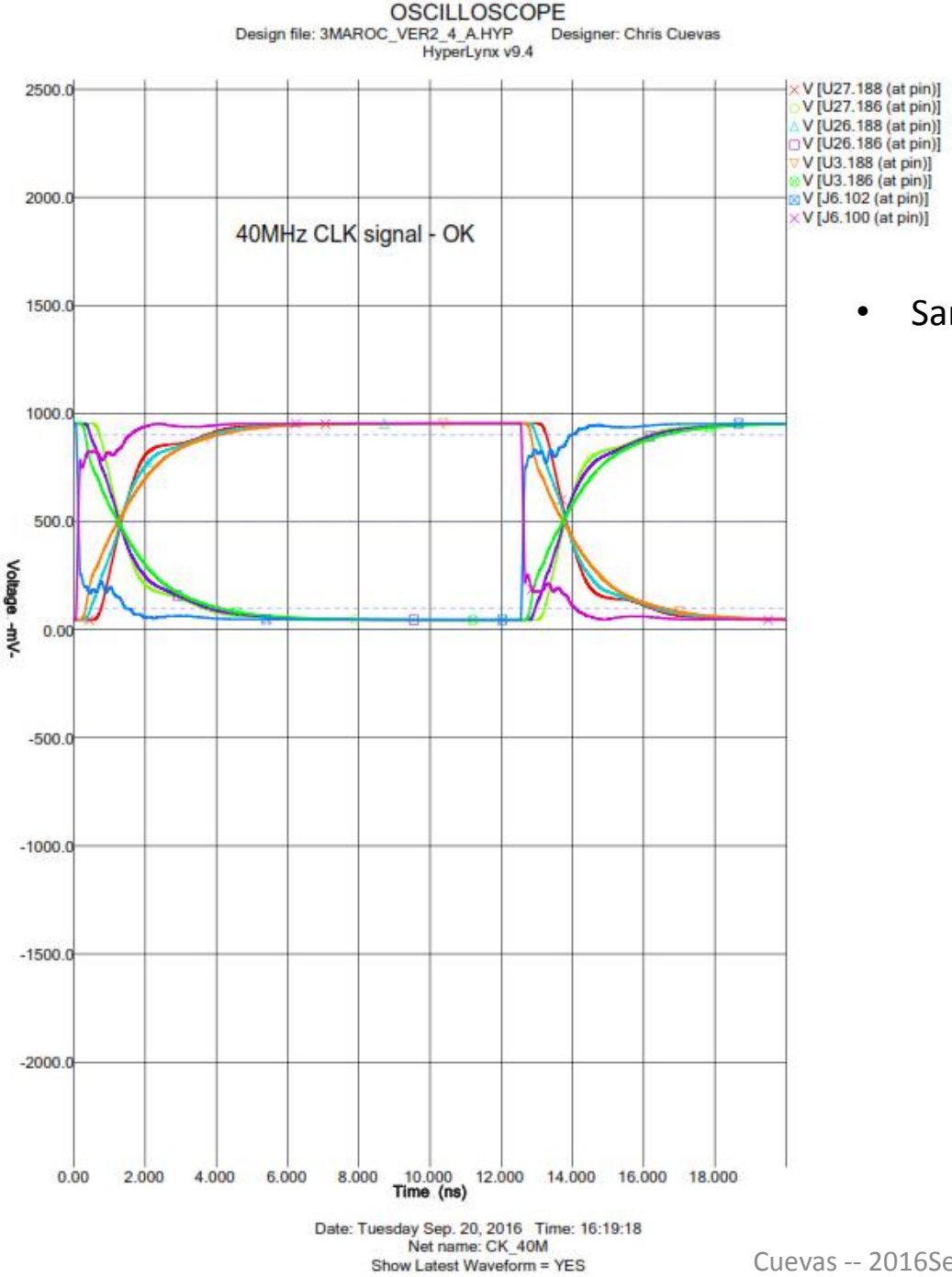
MID4



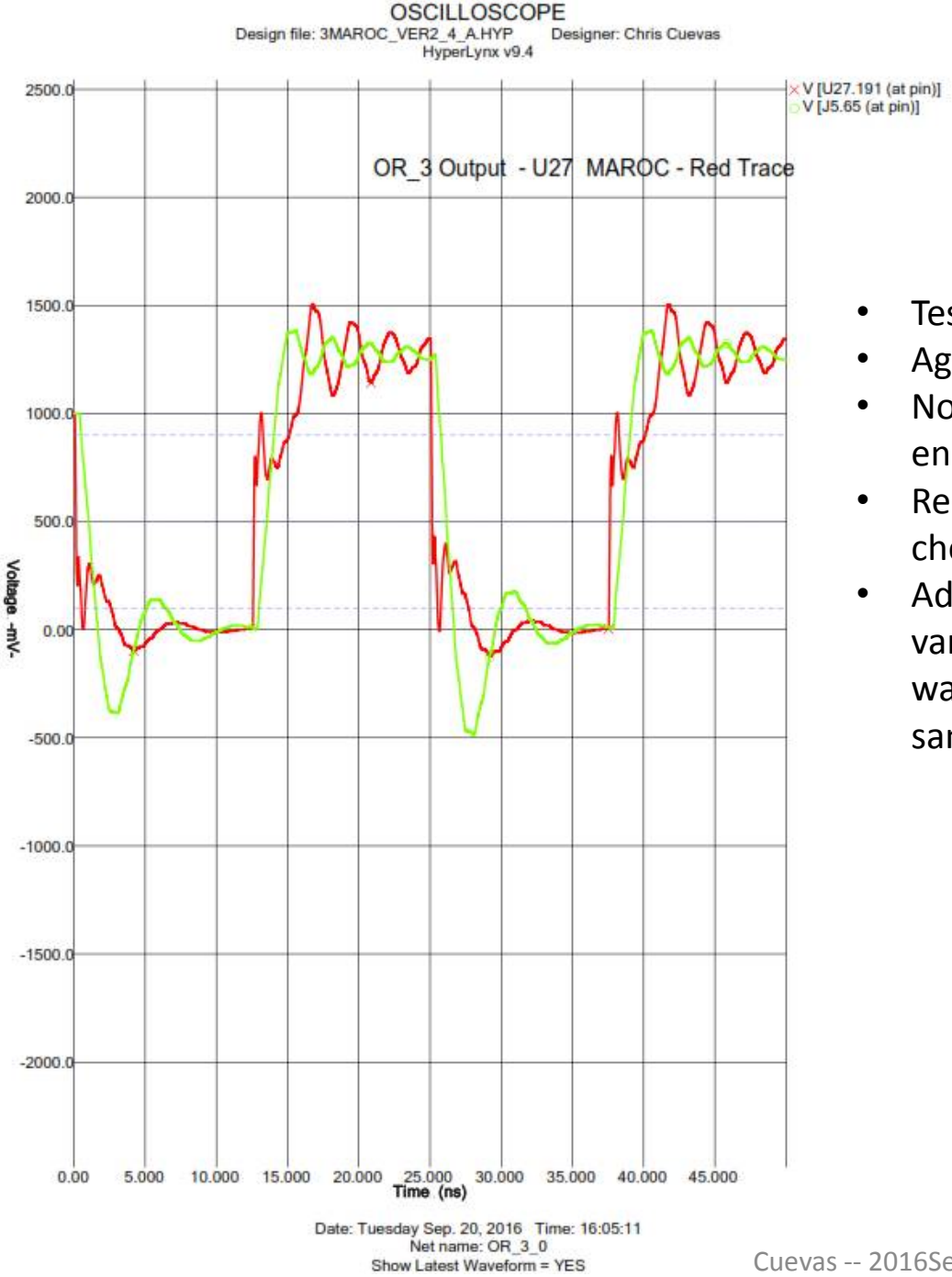
- Digital outputs do not cross Analog input signal traces

- Mostly Analog input signal traces
- Adapter board connectors mounted to bottom of PCB

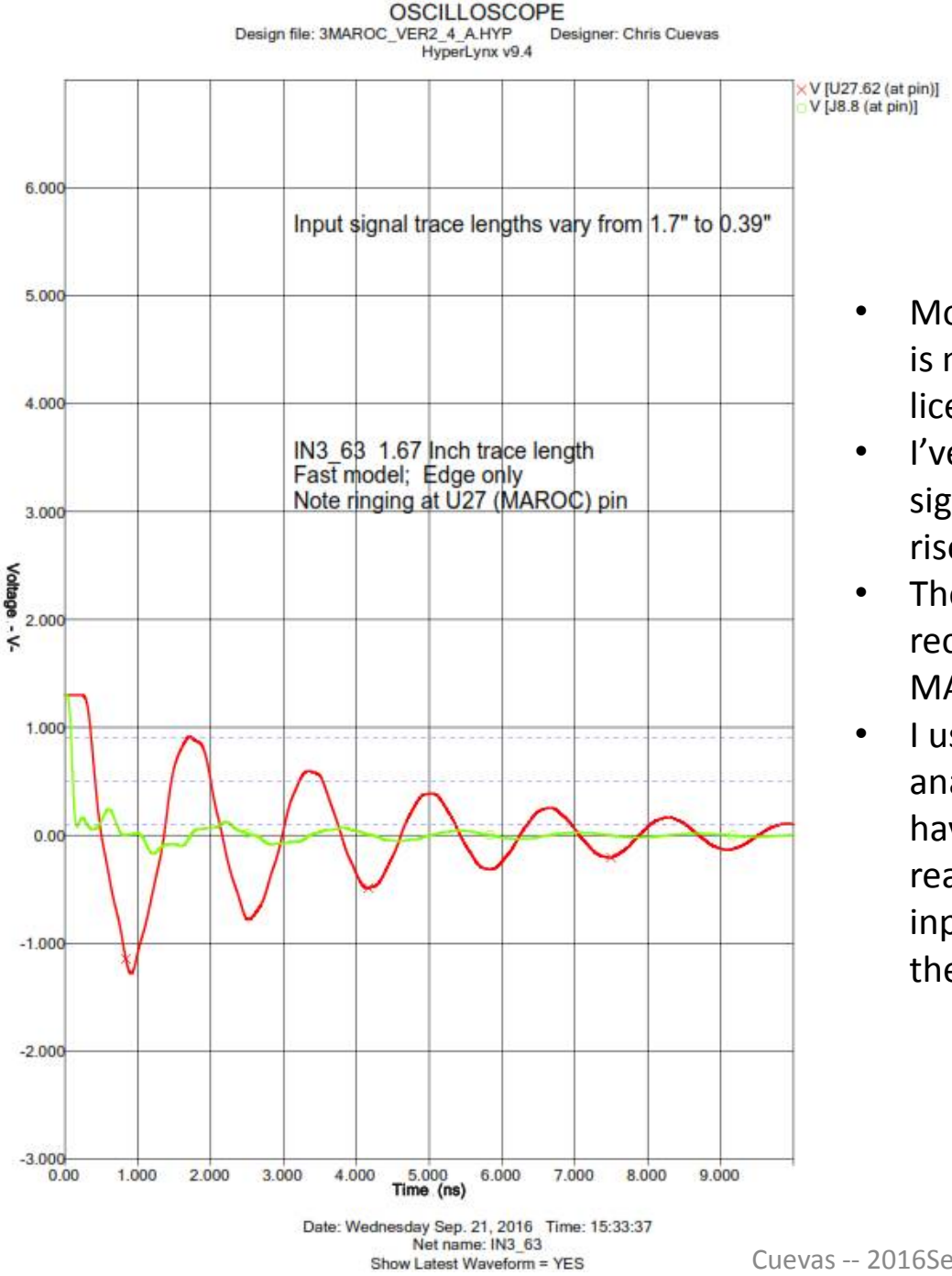




- Sanity check with modeling tool
  - -- Using a TDR style model with very fast rise time
  - -- Response looks reasonable
  - -- I may not have layer stack setup exactly, but this result makes sense



- Test of OR output
- Again, very fast model for driver
- Note ringing and undershoot at receiver end.(J5 connector)
- Result is fine and provides another good check on digital lines.
- Adjusting driver model and layer stack variables would probably improve response waveform, but this model test is a good sanity check.



- Modeling the Analog pulse from the maPMT is not so easy given that our HyperLynx license only supports IBIS models.
- I've used a single fast edge model as the signal source that would mimic the fast risetime of the tube output.
- The ringing(red) is probably because the receiver model is not anything like the MARAC3 input.
- I used one of the longest input lines for this analysis, and the layer stack variables may have a small impact, but the ringing is not realistic. Will require adjustment to the input signal model to simulate a signal from the maPMT.

Summary

- Version 2_4_a layout appears to definitely attack issues with digital output signals influencing the low level analog input traces.
- Digital lines have clearly been moved away from Analog input traces and separated on several layers.
- Addition of Analog return(GND) copper is also noted and will definitely improve signal quality and isolation from digital influence.
- Modeling a few digital lines with HyperLynx was worth the effort, and the use of exact models for the MAROC3 drive/receive variables was simulated with generic TDR driver/receiver models.
- Input signal crosstalk should be simulated and models will have to be adjusted to properly simulate a charge pulse driven from the maPMT. Present layout shows fairly long input signal lines very close to other input lines, so it would be good to model for sanity check before fabrication.