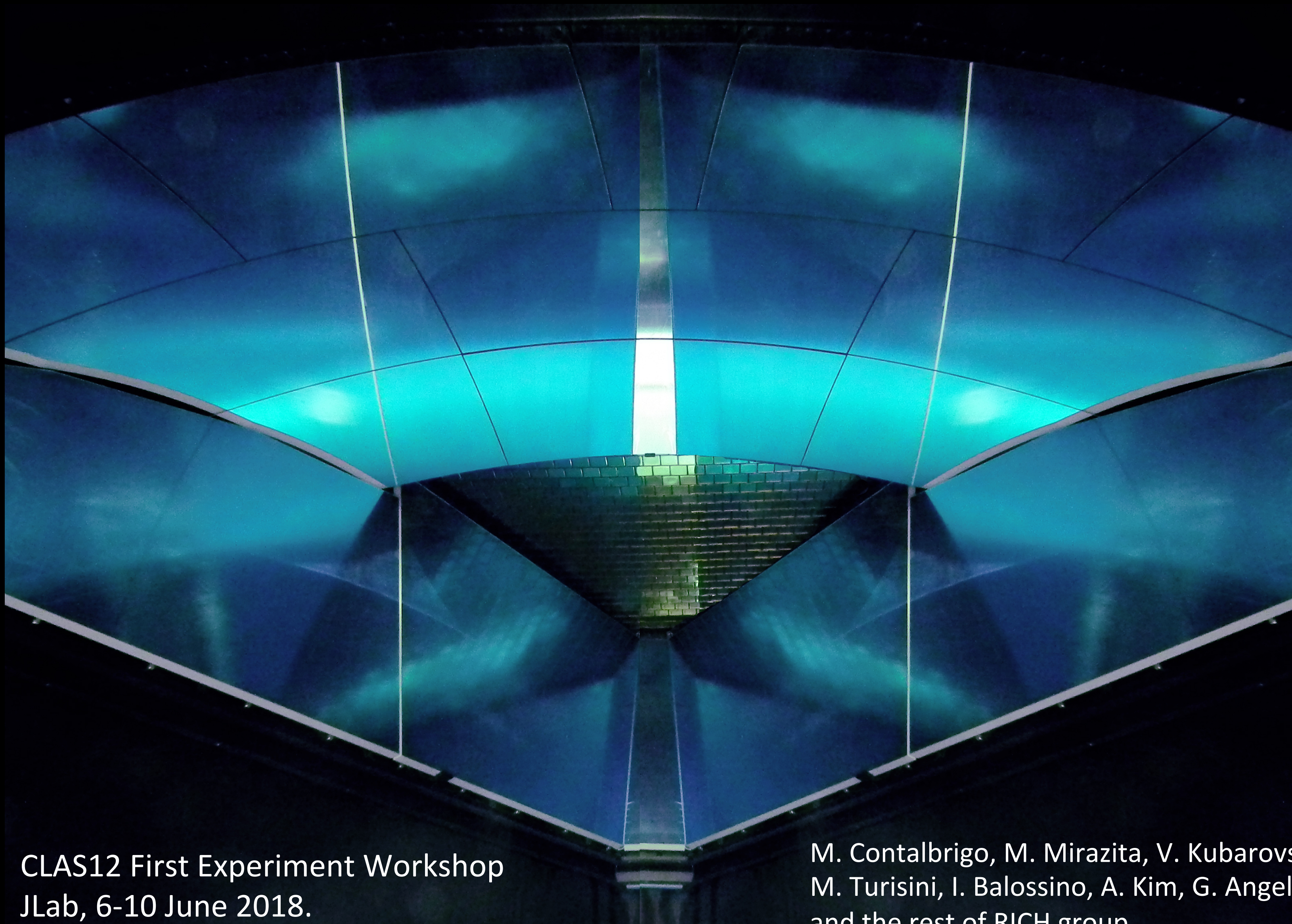
RICH detector settings, calibration, performance – status and plan

M. Contalbrigo – INFN Ferrara

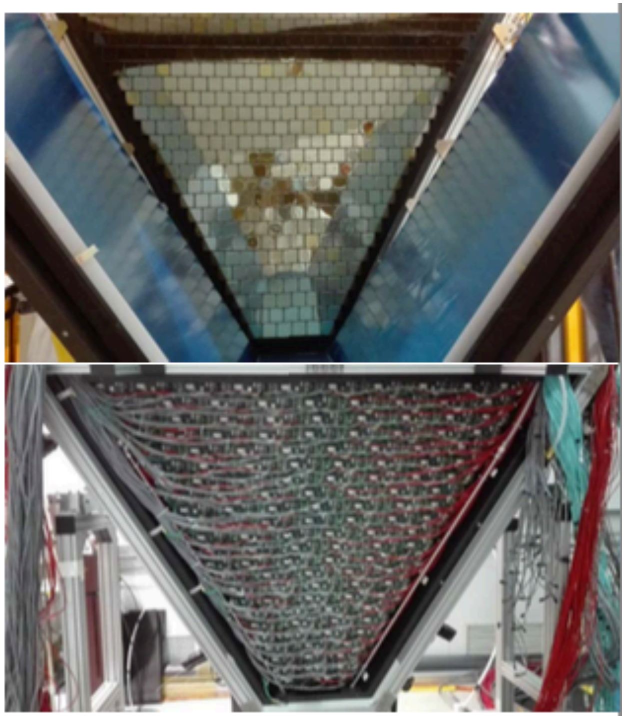


CLAS12 First Experiment Workshop
JLab, 6-10 June 2018.

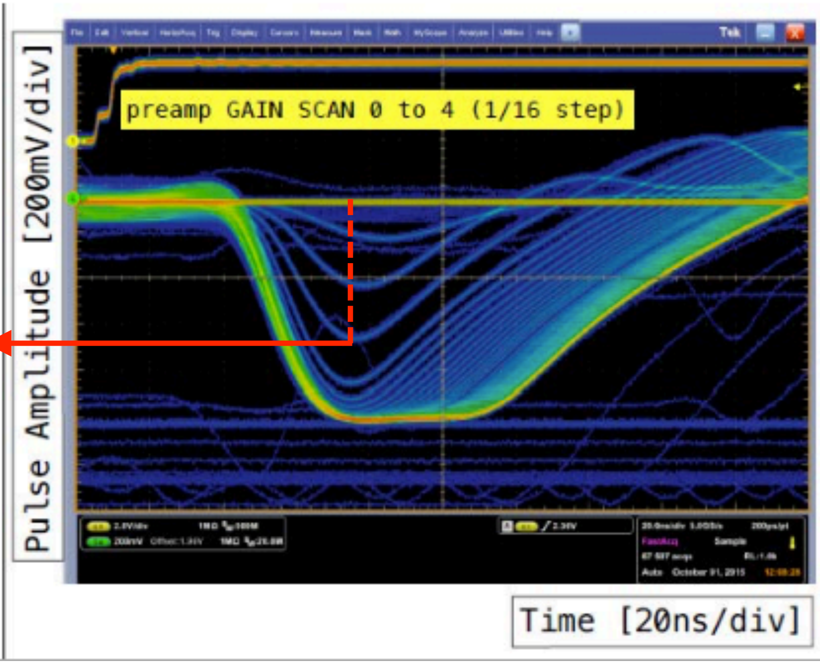
M. Contalbrigo, M. Mirazita, V. Kubarovsky,
M. Turisini, I. Balossino, A. Kim, G. Angelini,
and the rest of RICH group

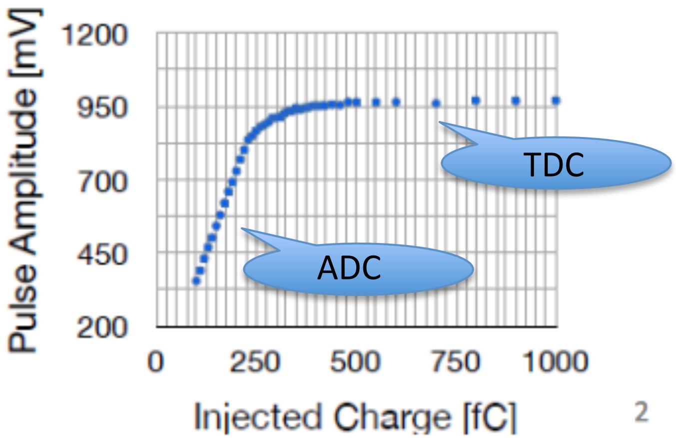
RICH Readout

- **391 MultiAnode PMTs grouped in 138 tiles (x2 or x3)**
- **One FPGA board configures and reads out each tile**
- **One MAROC chip per MAPMT**
- **Binary readout on 25024 independent channels (no ADC)**



Fast shaper and preamplifier on each channel
- Non-linear behavior already at fraction of p.e., optimal for 0/1 response

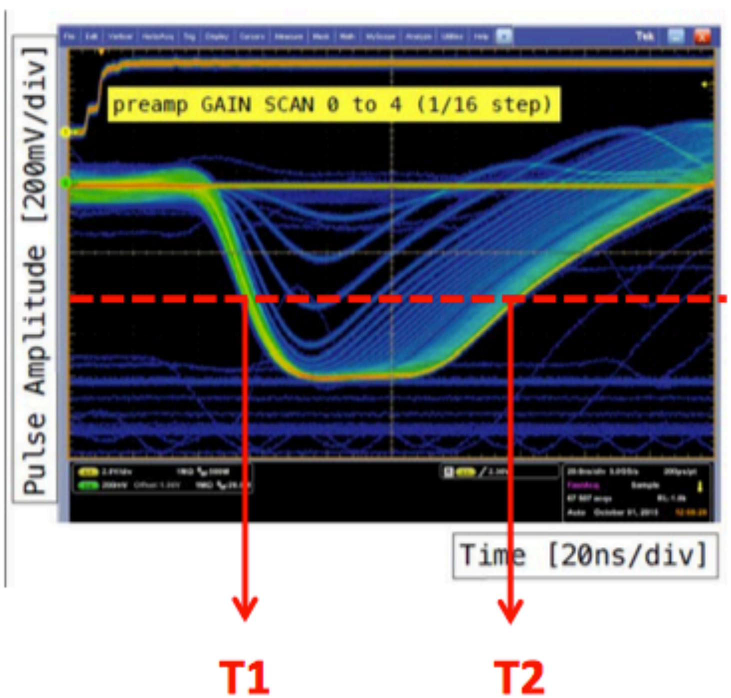


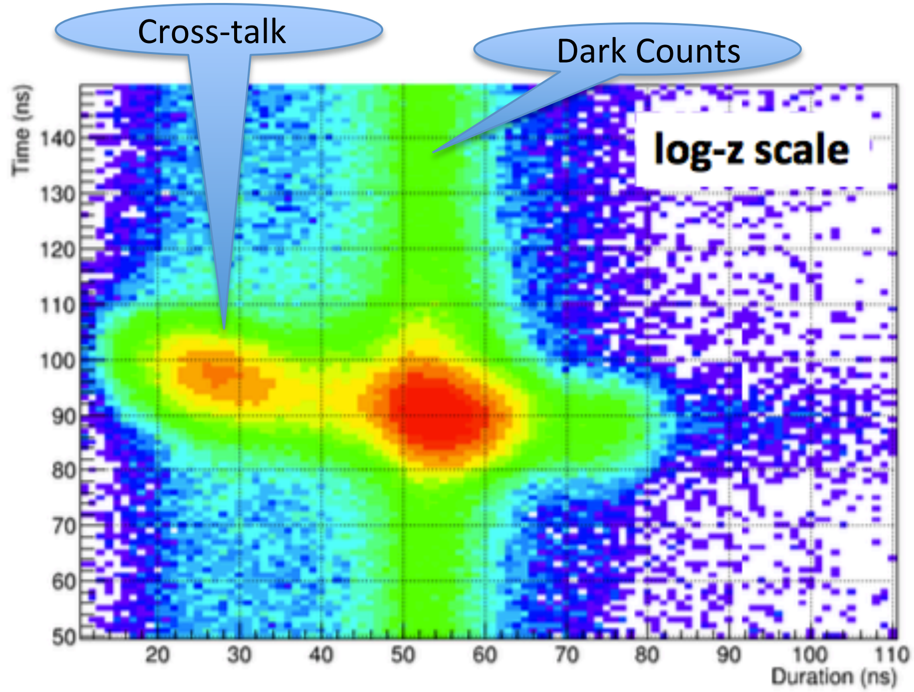


RICH TDC Readout

HIT reconstruction

- The FE electronics provides for each pixel the list of times at which the signal crossed the threshold
- each time is marked as leading or trailing edge
- a reconstructed hit is made by a leading edge (T1) followed by a trailing edge (T2)
- T1 provides the time resolution, T2-T1 the duration of the hit, which is proportional to the charge





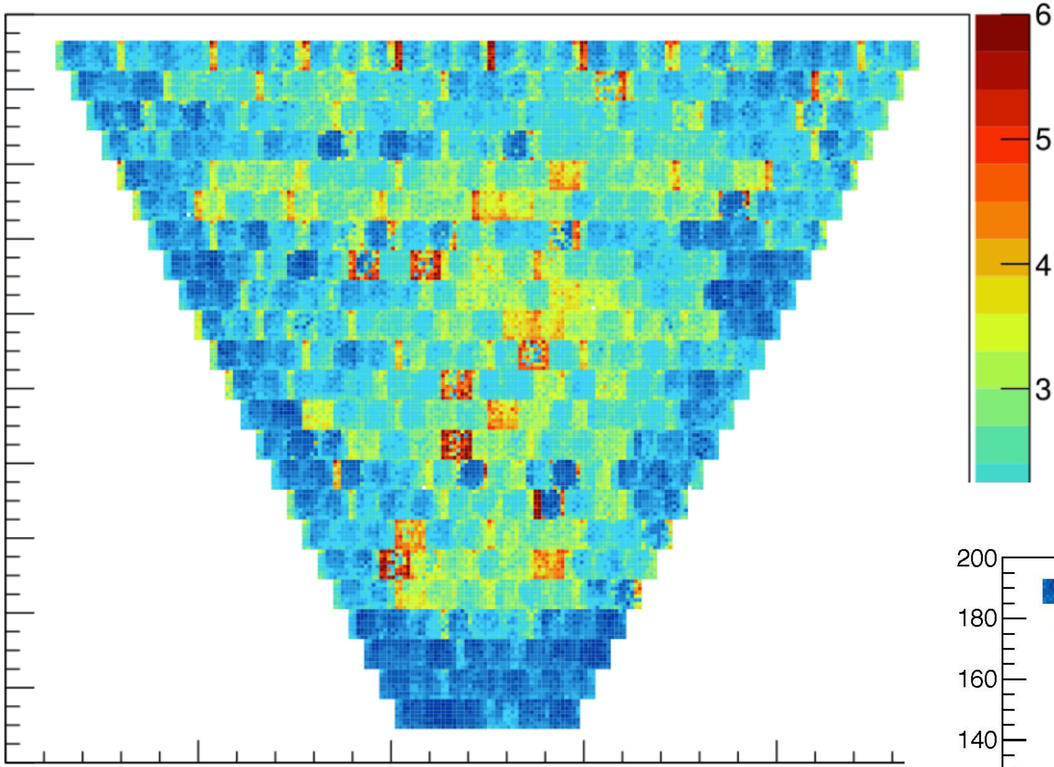
RICH Commissioning and Calibration

1) **Data Acquisition**
   - FE gain, one per channel: 25024 parameters
   - FE threshold, one per MAPMT: 391 parameters

2) **Event reconstruction**
   - channel-to-channel time offsets: 25024 parameters
   - time walk correction: 391 functions

➢ **Stability monitoring tools**
- Pedestal runs -> baseline, dead channels
- Dark runs -> hot pixels
- LED runs -> time offsets, time-walk correction
- physics data

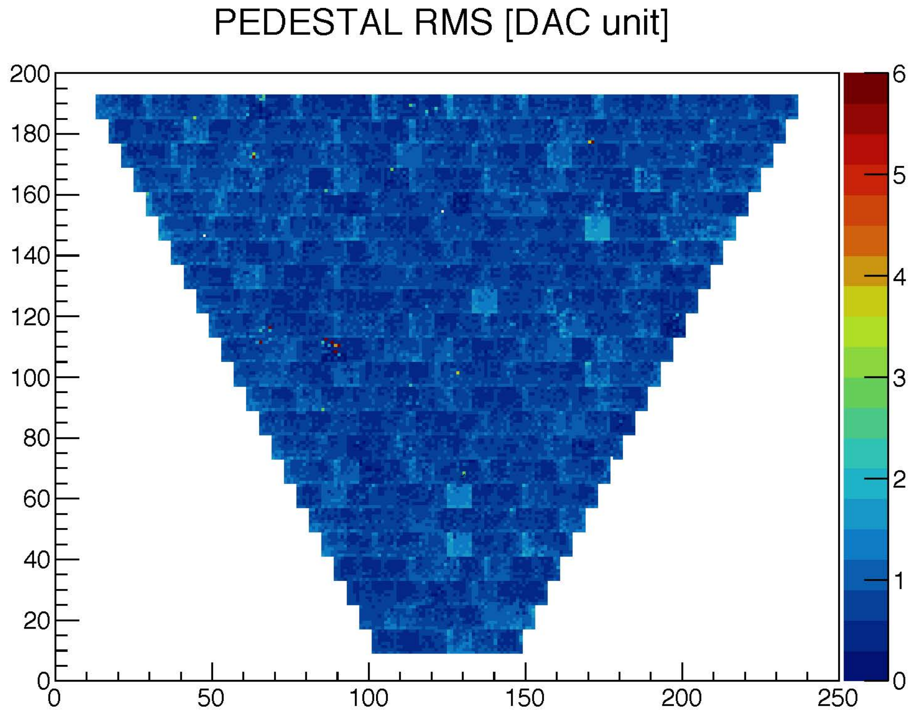
Pedestal RMS Distribution



TDC discriminator baseline

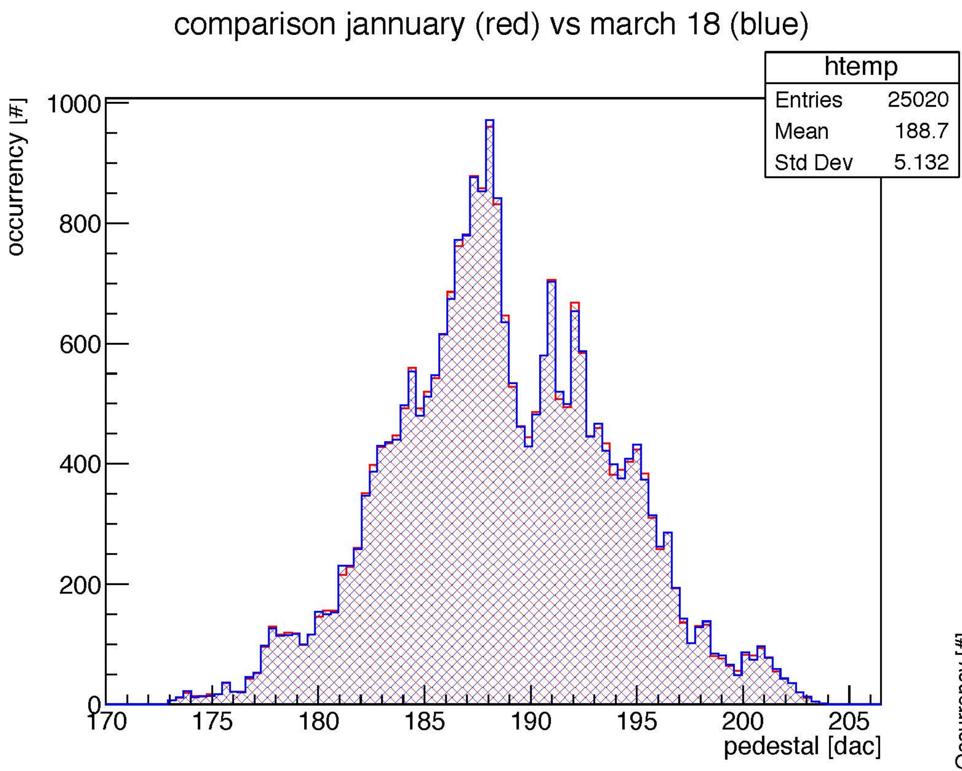
1 DAC ~ 1 mV

Typical single-photon signal around 400 DAC



Grounding grid with jumpers between boards improved the situation

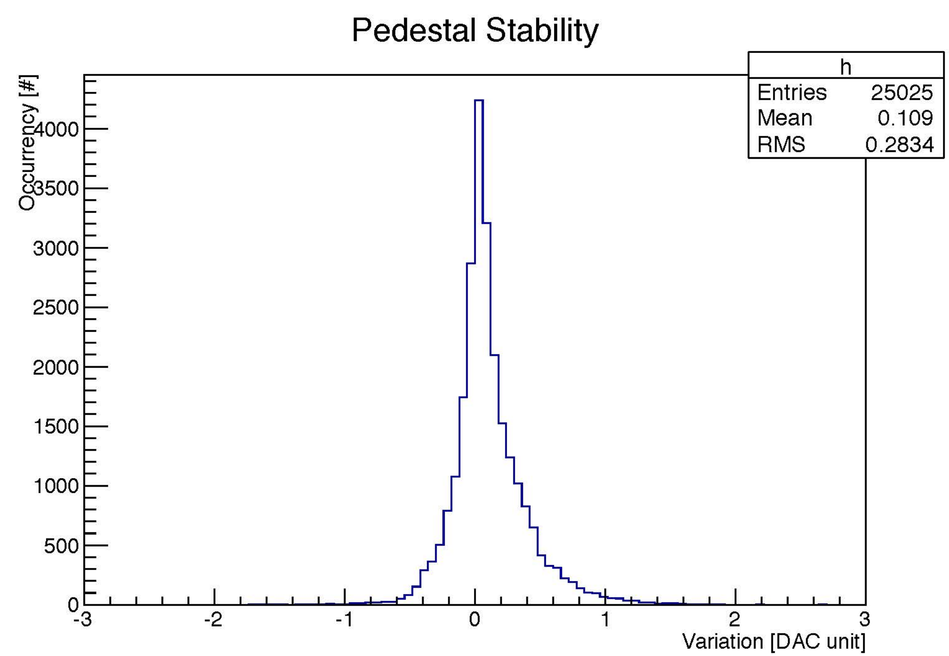
Pedestals Stability



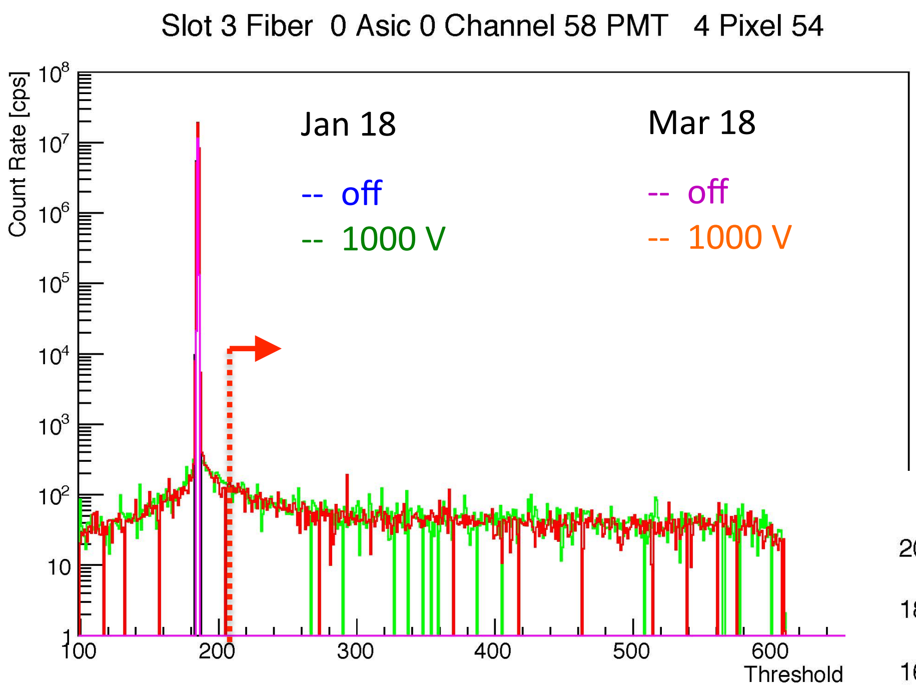
Pedestal measured for each active channel

~ 1fC/DAC, ~ 500 fC/SPE

Negligible variation with time

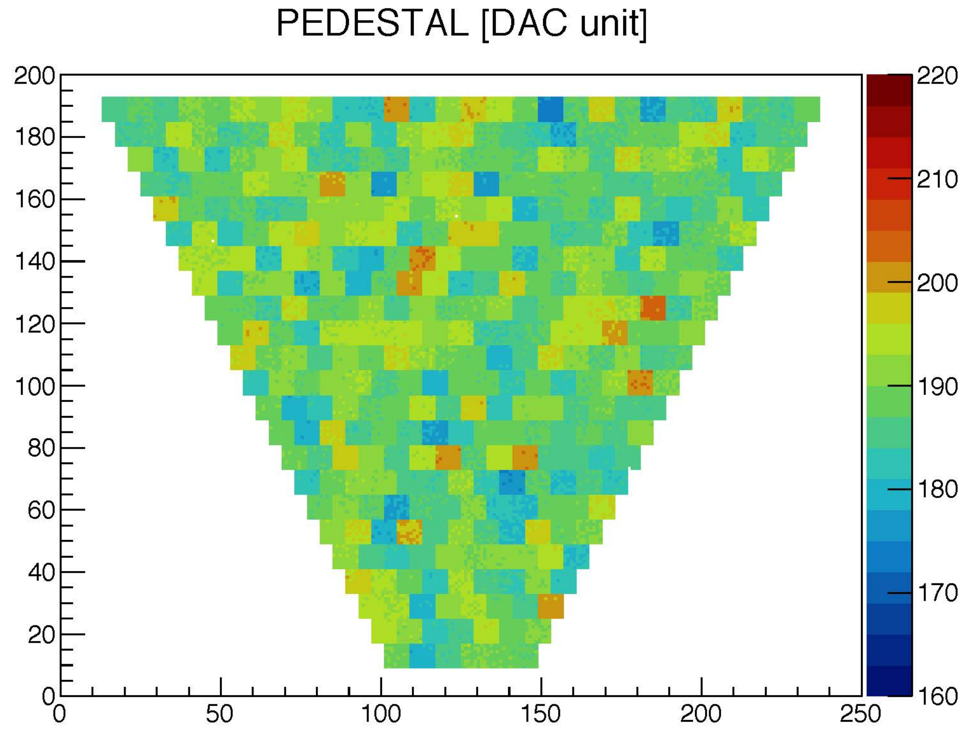


Pedestal vs Threshold



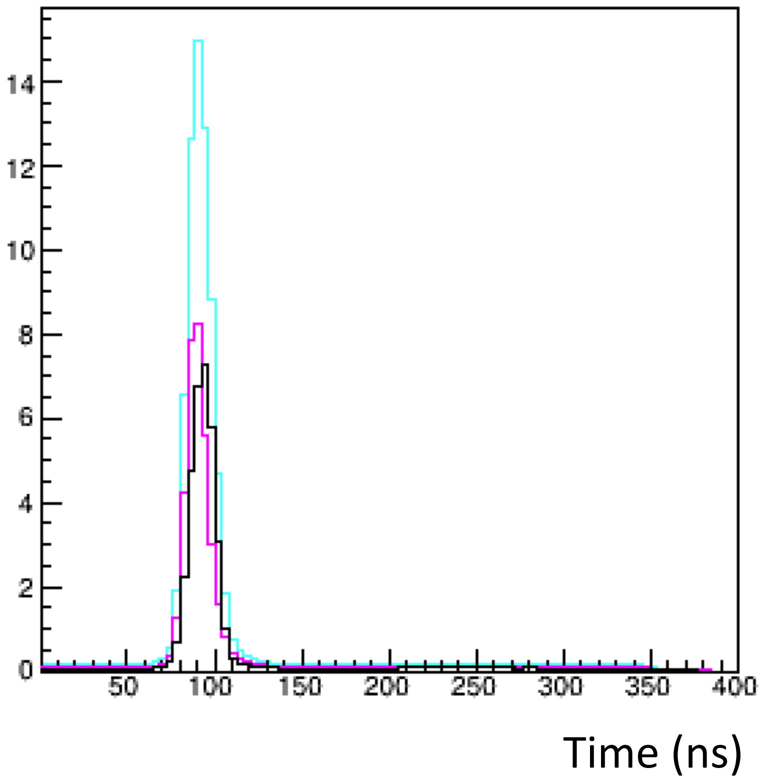
SPE saturated signal ~ 600 DAC

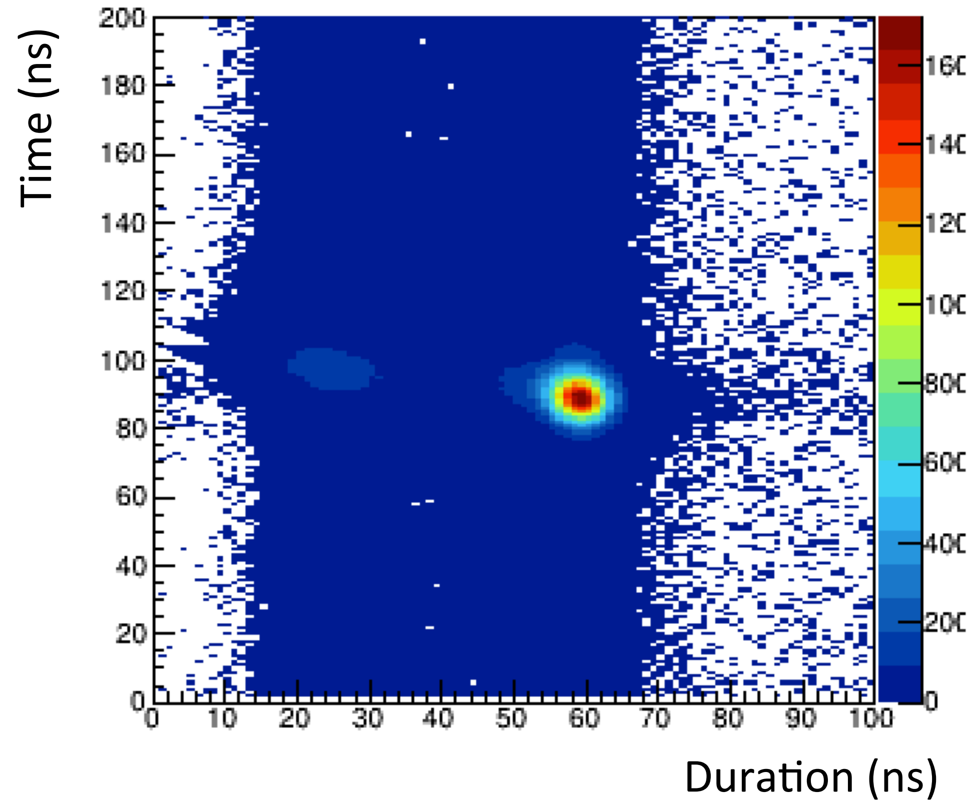
Average pedestal of the chip used to define the threshold, i.e. +25 DAC



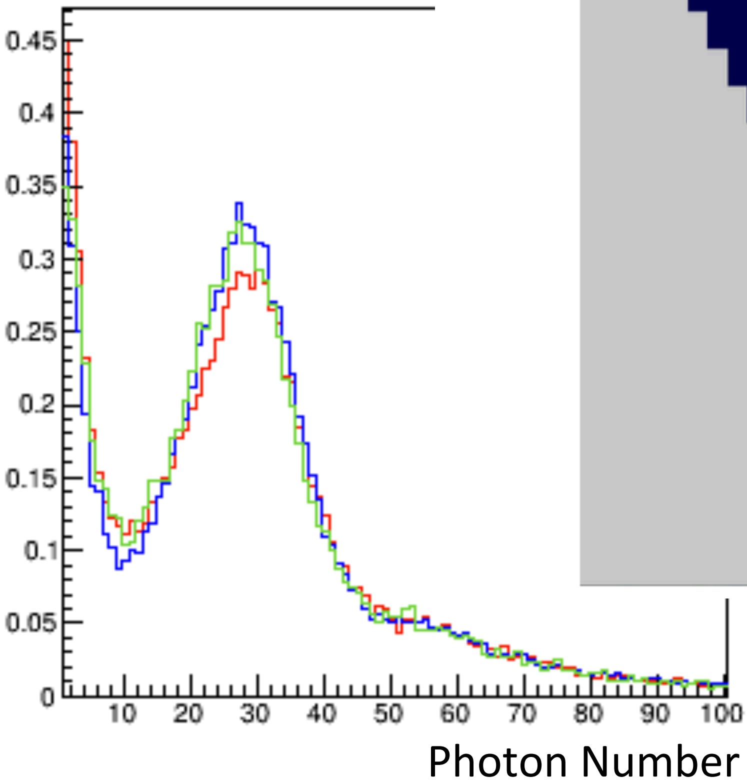
RICH Timing

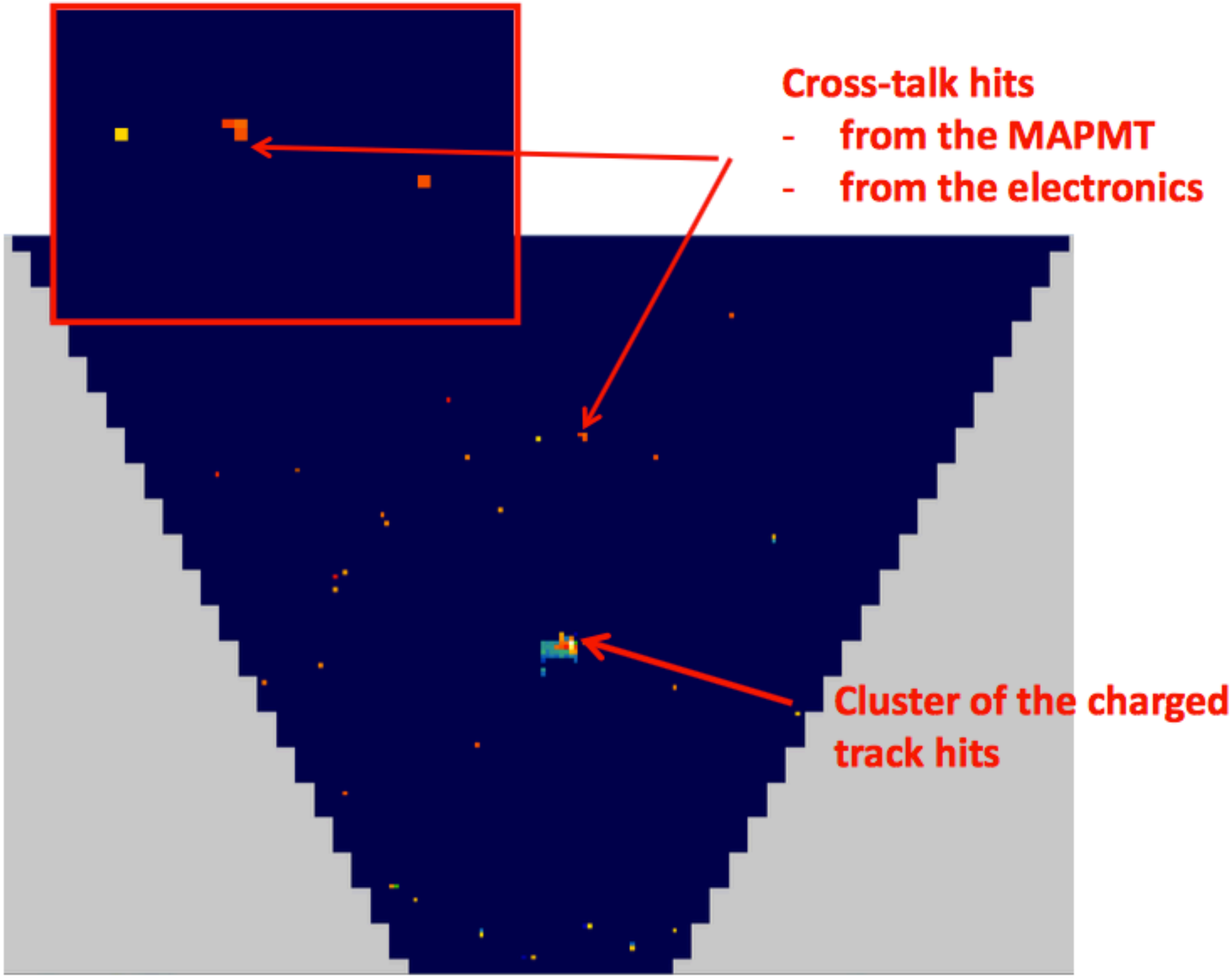
Readout time window well defined (during engineering run)





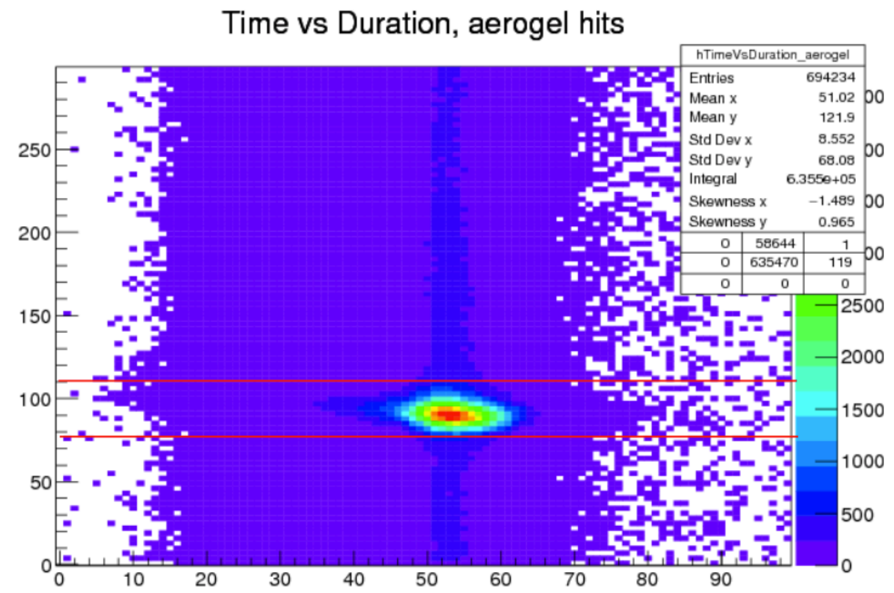
RICH Hit Classification

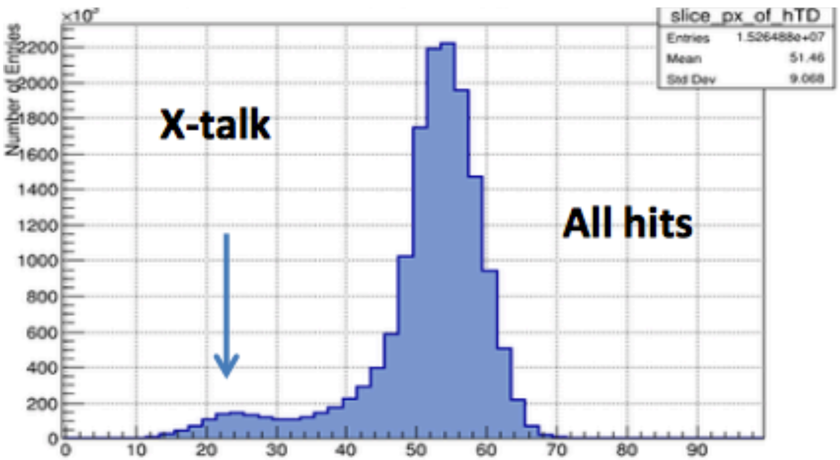


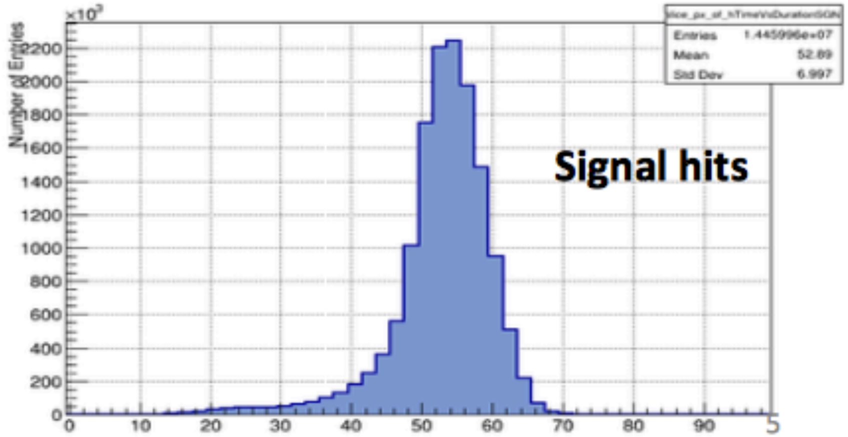


Single Photo-Electron Hits

Hit digitalization and
cluster reconstruction
released and added to coatjava

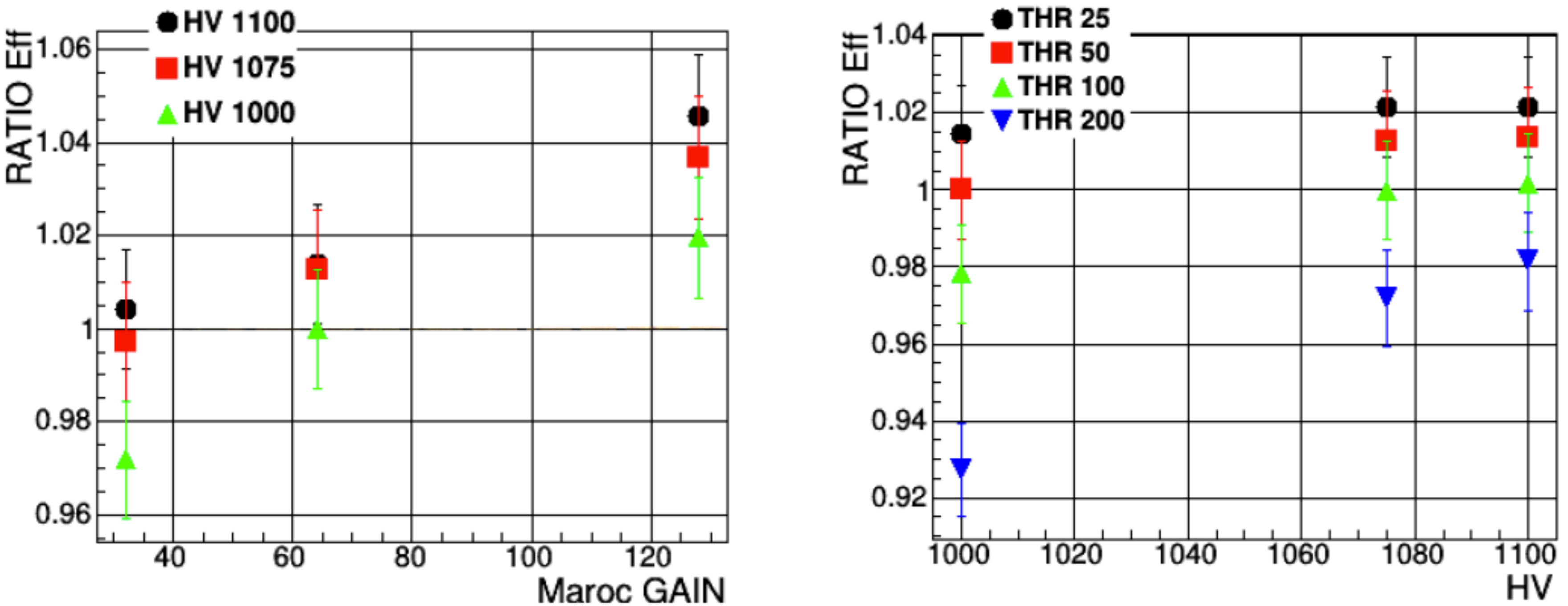






RICH Working Range

Relative efficiency as a function of the working parameter

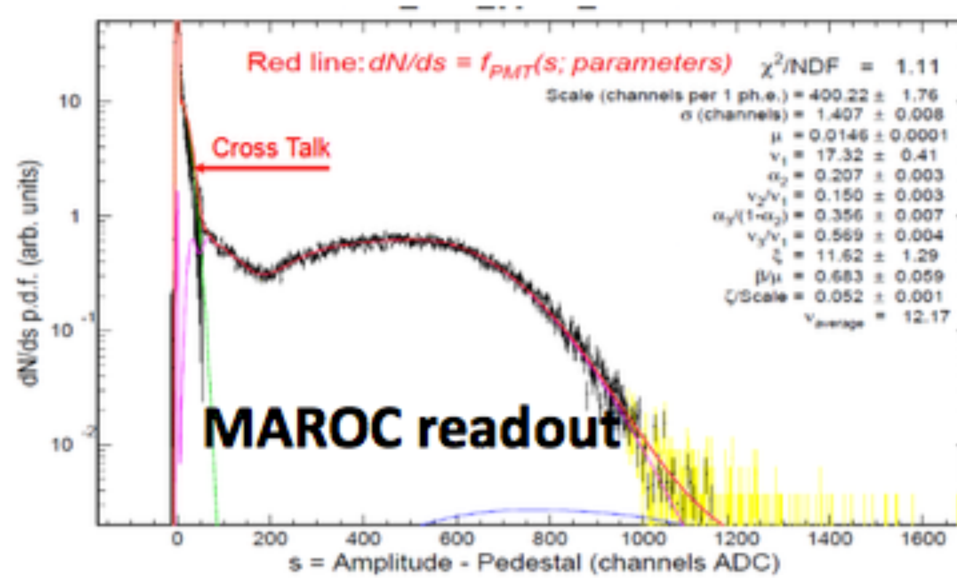


Ranges:	HV	[1000 – 1100]	Volts
	MAROC Gain	[32 – 128]	Bits (64 means x1)
	MARCO Thr.	[25 - 200]	DAC (SPE typical signal around 500 DAC)

Calibration and Monitoring Tools

Results from the MAPMT characterization tests with a laser have been used to select best working point

- HV 1000 Volt
- Threshold +25
- Gain equalized



Special test runs have been taken

TEST1: 1/30/2018

- **MAROC gains calculated to equalize the average SPE charge**
- **three sets of thresholds (low, intermediate, high)**

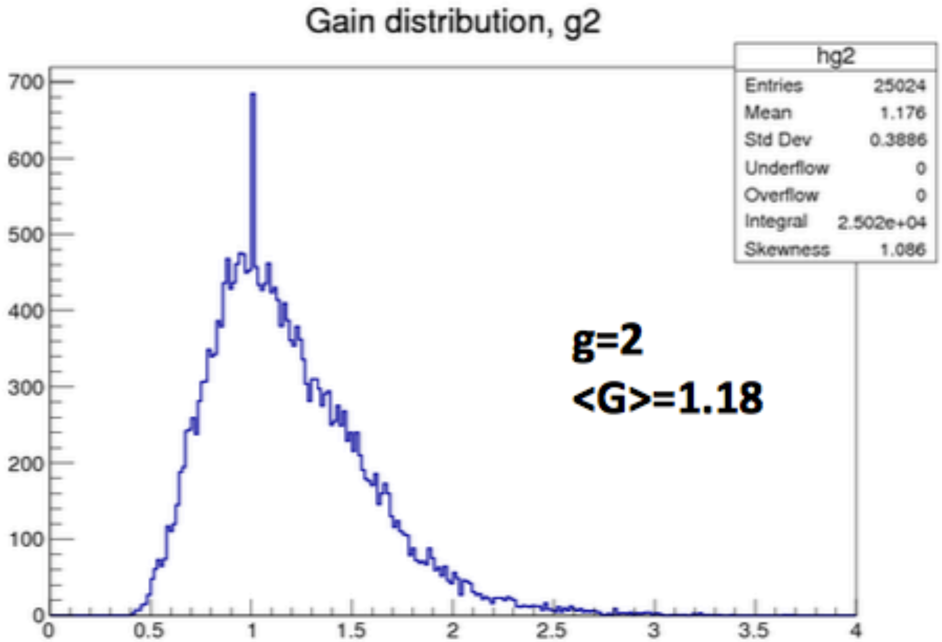
TEST2: 2/14/2018

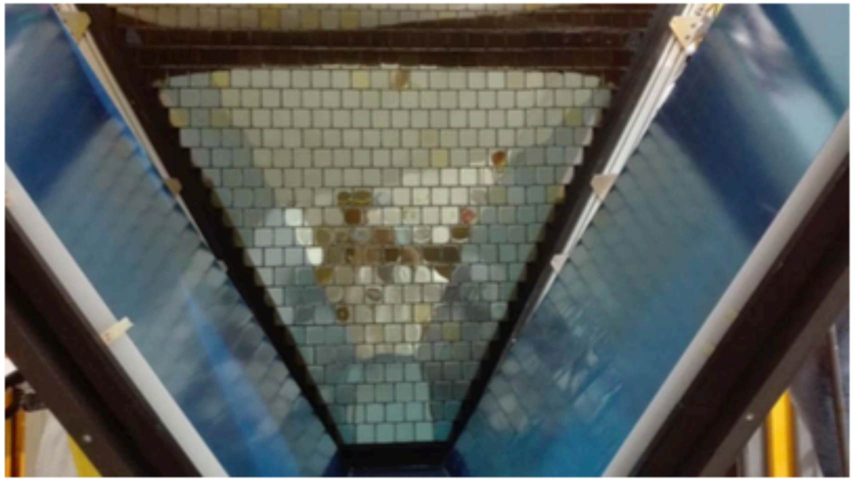
- **MAROC gains and thresholds set to equalize the cross-talk contamination and the average SPE charge**
- **Various sets tested, different HV values**

Gain Setting Test1

Before equalization: all gains set to 1

After equalization: average gain close to 1, values between about 0.5 and 2.5





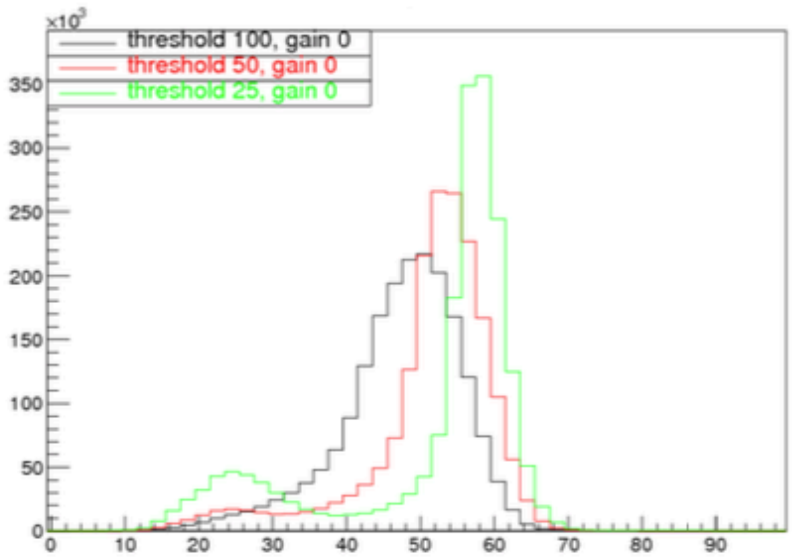
- **MAPMT close to the beam line:**
  Higher MAPMT gain -> MAROC gain below 1
- **MAPMT at larger angle:**
  Lower MAPMT gain -> MAROC gain above 1

Gain Setting Test1

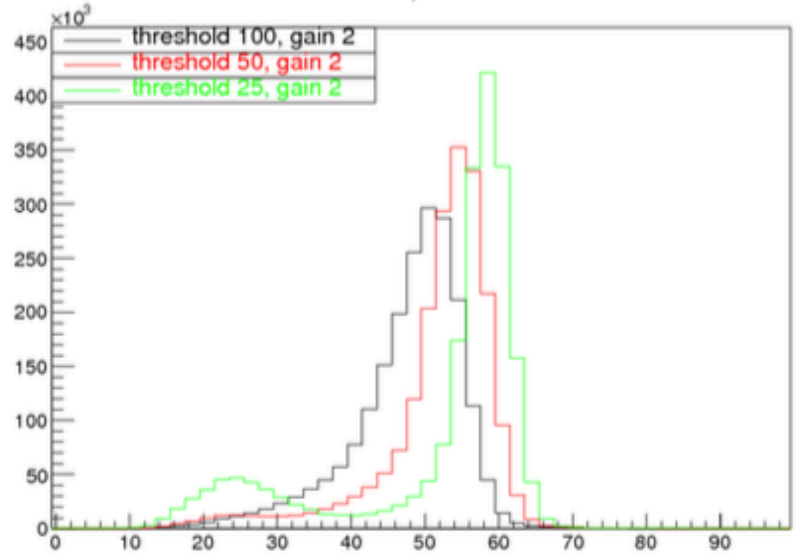
Duration distributions, all the channels and PMTs

black: high threshold **red: intermediate threshold** **green: low threshold**

Before equalization



After equalization



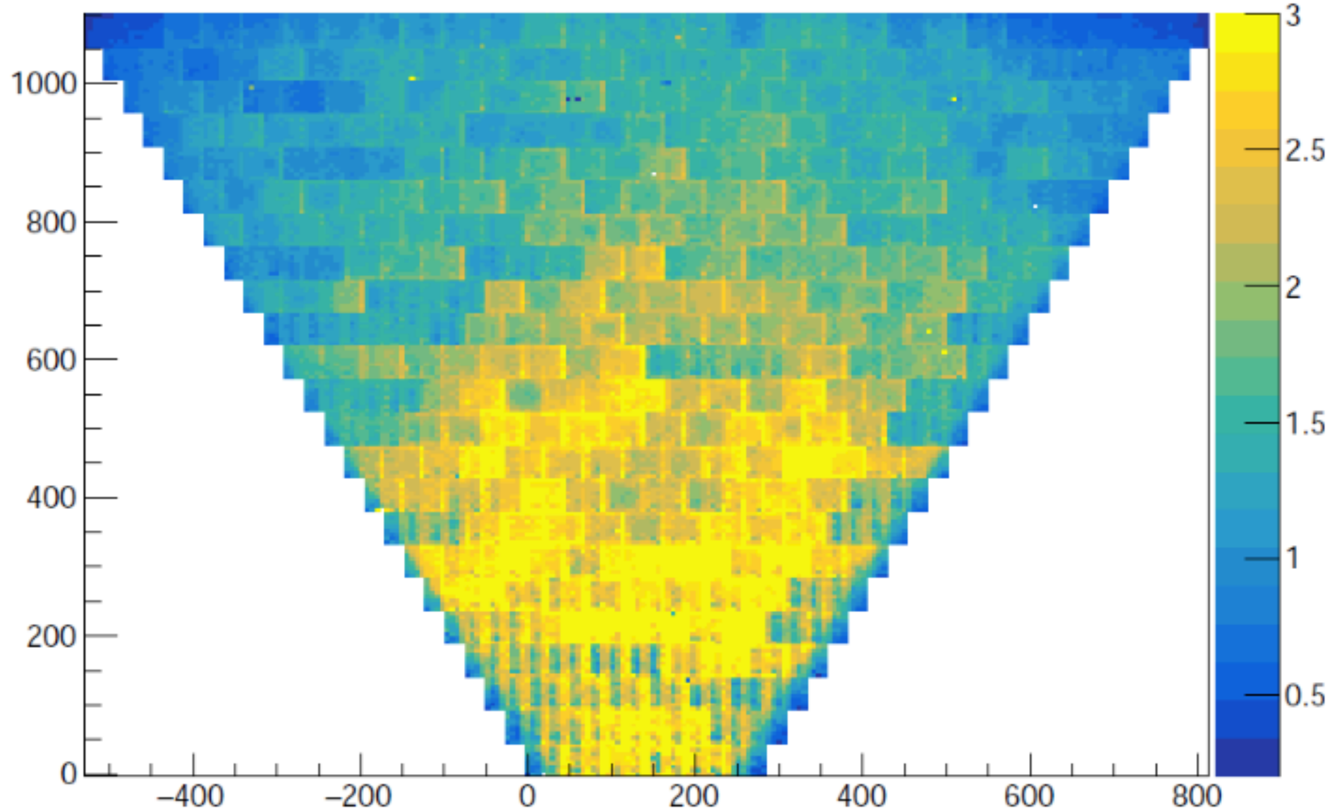
- **After equalization the distributions are less sensitive to the threshold**
- **Higher thresholds cut the tail of short signals**

Efficiency Study

Three MAPMTs with no gain change have been used to normalize the counts

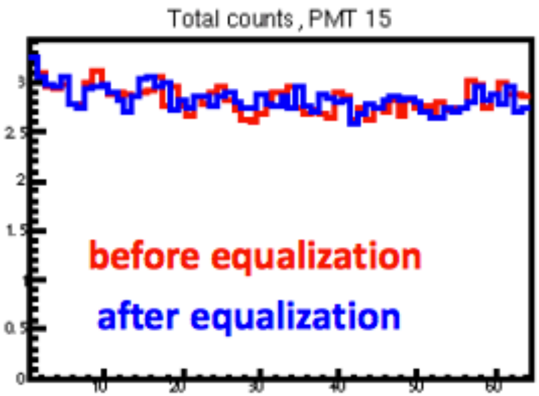
$$N_{norm}(c) = N_{raw}(c) / \langle N_{raw}(c, MAPMT=83,203,314) \rangle$$

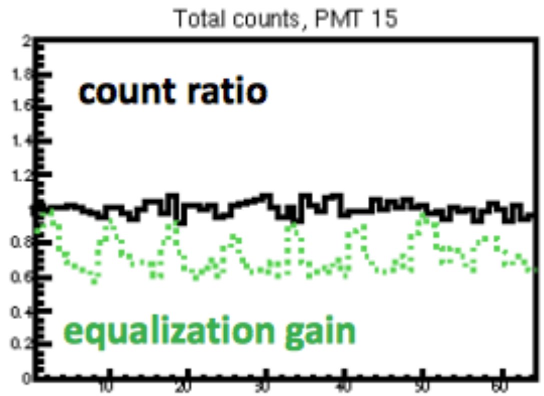
Normalized counts have been compared with different running conditions



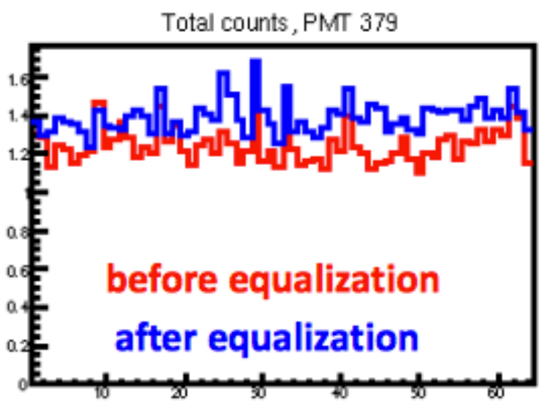
Gain Equalization

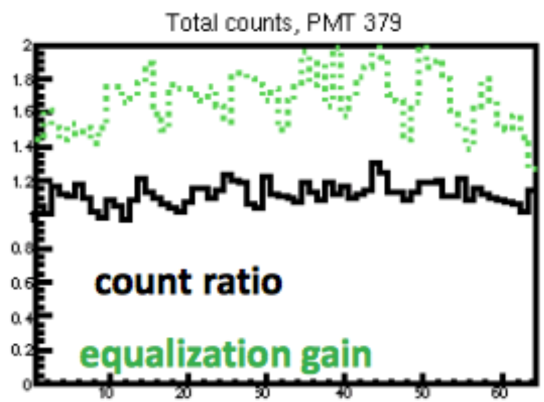
Test done at high threshold





Forward MAPMT
Equalization gain below 1 but no change in the efficiency

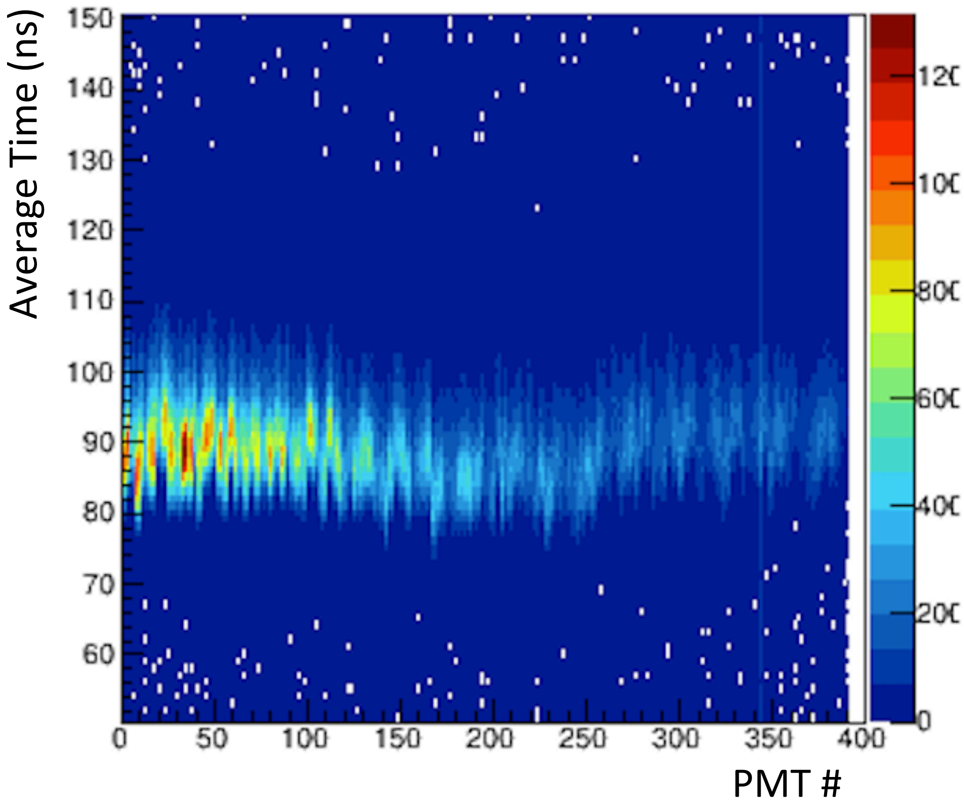




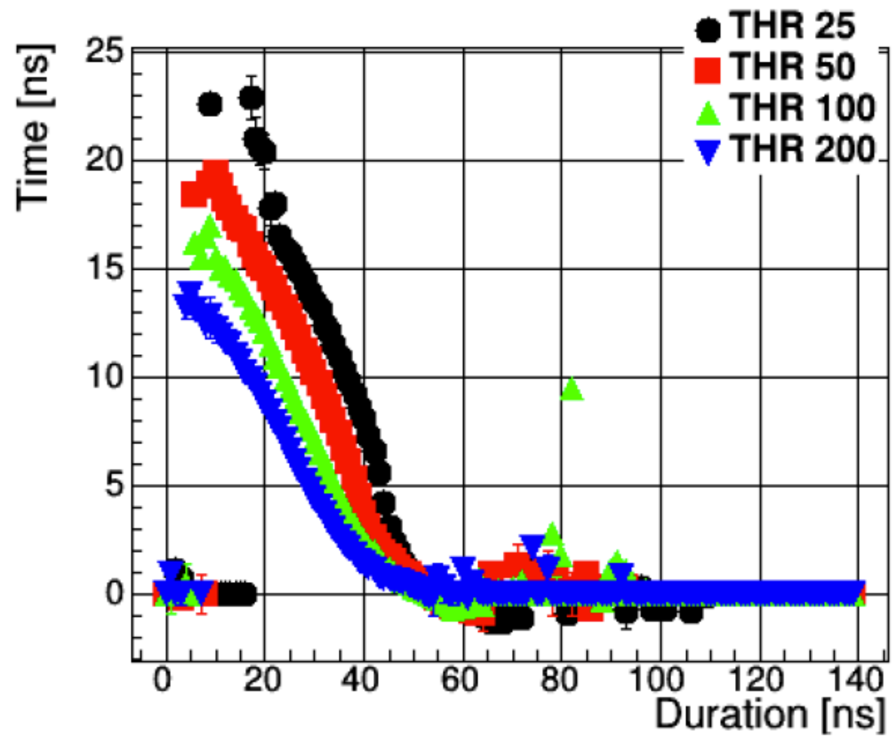
Large angle MAPMT
Equalization gain between 1.5 and 2 but less than 15% increase in the efficiency

Time Calibration

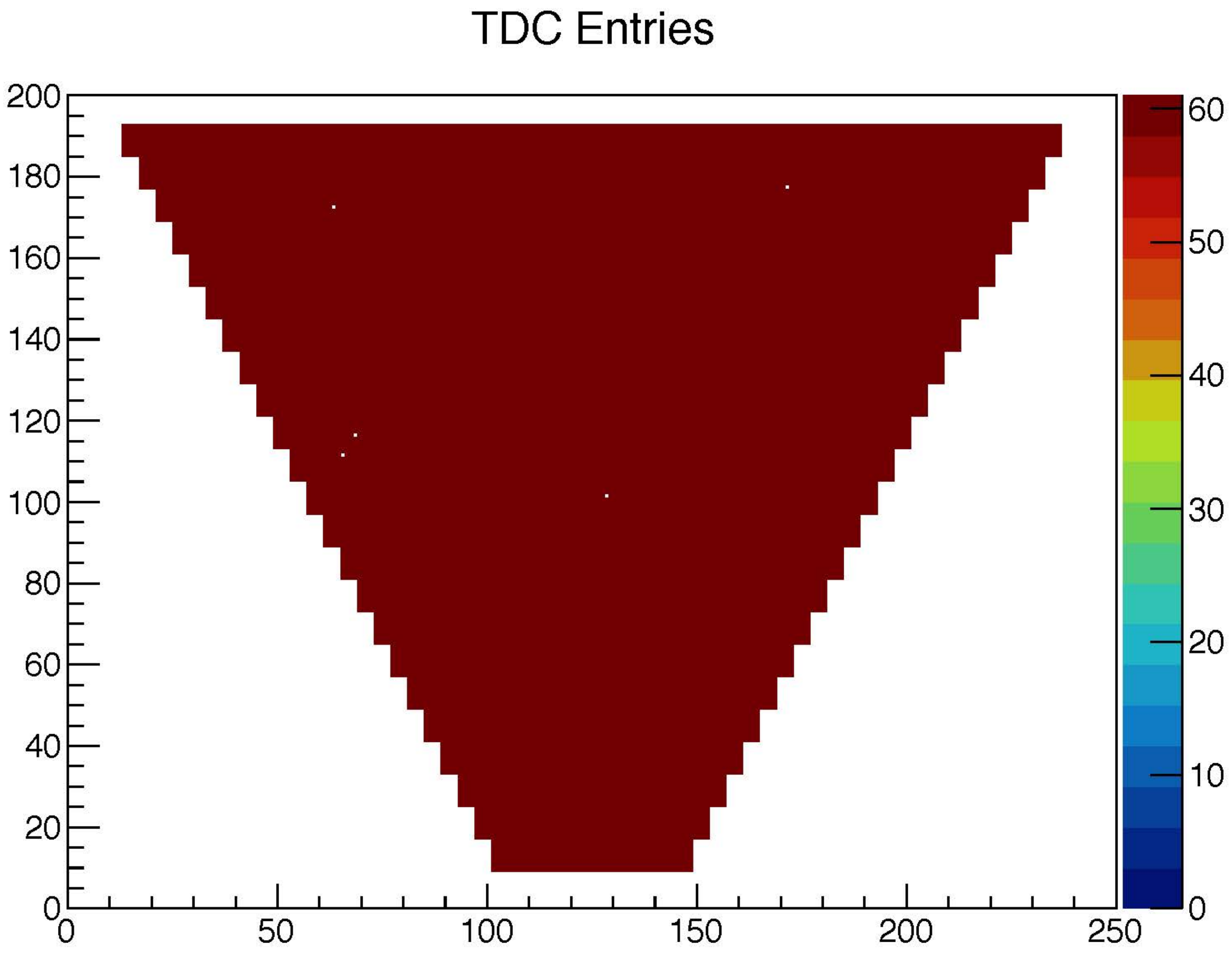
Time offsets from real data
LED system



Time walk from laser stand
LED system



Dead Channels



DAQ Troubleshooting

It occurred few times during the configuration of the run that the RICH readout was not correctly set up

1) **The optical link with one FPGA is lost**
    - **Data taking may or may not start regularly. An alarm was generated**
    - **The problem has been solved (hopefully) by making the FPGA discovery process more robust**
2) **A MAROC chip is not recognized by the FPGA**
    - **The connection with the FPGA is ok, but the tile is not taking/sending data**
    - **A fix has been implemented**

The origin of the problem is not clear yet, it might be due to a firmware bug or to radiation damage.

Usually a LV power cycle solve the problem.

Conclusions

➢ **The RICH is taking data since the beginning of RGA with equalized gains and low thresholds, HV=1000 V**

- 5 **dead channels**
- **7 hot pixels**

Next steps

1) **Refine the efficiency studies: individual channel time cuts, background subtraction, etc.**
2) **Analyze the data from TEST2: in progress**
3) **Perform the time calibration on each channel**
4) **Implement correlations with other detectors**

Monitoring/calibration

We plan to take regular calibration and monitoring runs (~once per week)

- **pedestal and dark runs are fast**
- **LED runs might take few hours**