RICH Detector – Readout Electronics

DREAM ASIC

- 10mW/channel – **640mW (256W total)**
- 20KHz Trigger rate
- 50MHz ADC conversion/readout
- OR'ed 'Hit Bits'
- Package Type
  - LQFP 128 pins
  - 14mm x 14mm x 1.4mm
  - 0.4mm pitch

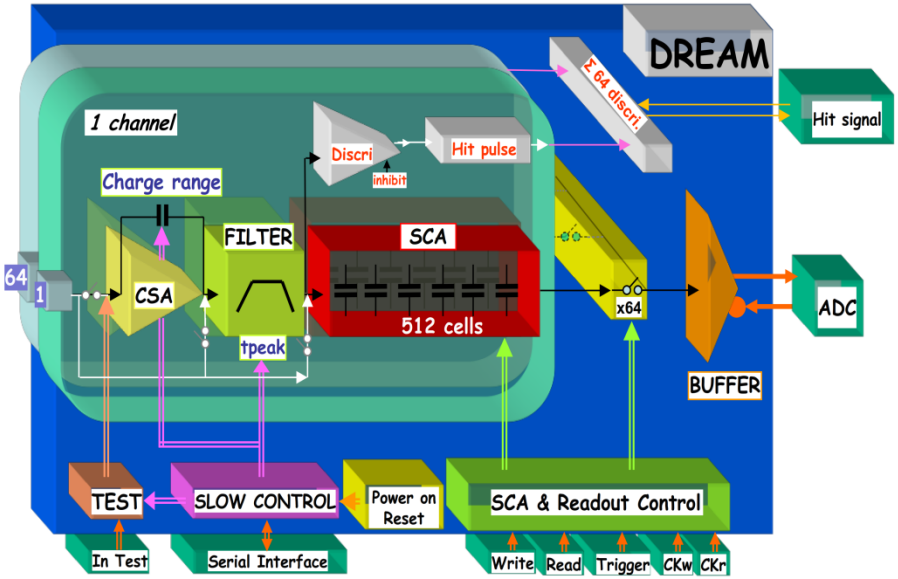
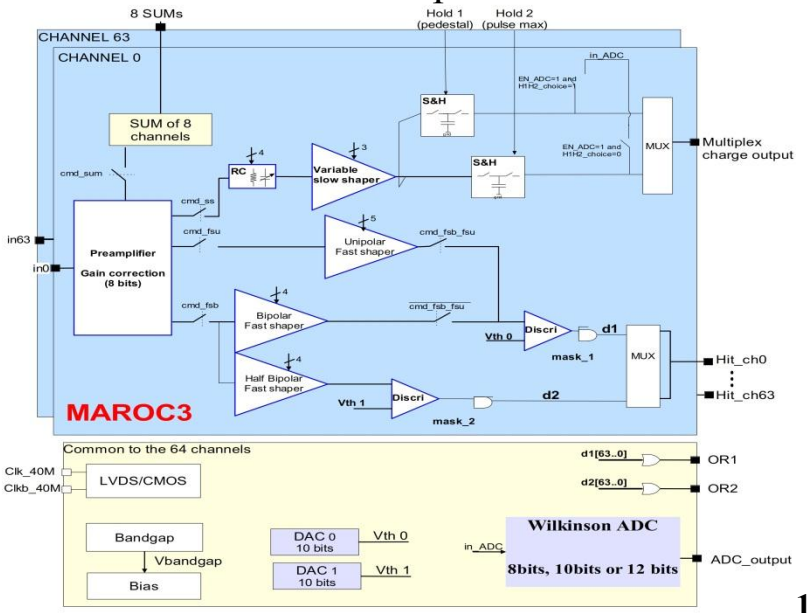


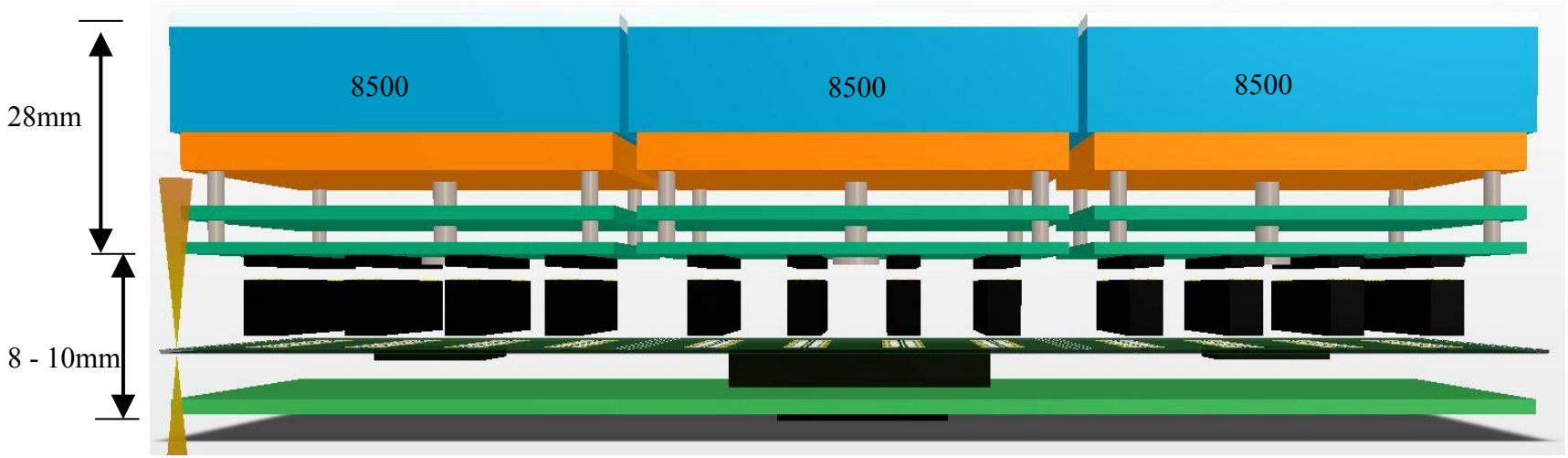
Fig. 1: Block diagram of the DREAM chip.

MAROC3 ASIC

- 3.5mW/channel – **224mW (89.6W total)**
- 64 'Hit Bits' TOT
- Sum of 8 output
- MUX'ed charge output
- Wilkinson ADC output
- Package Type
  - CQFP 240 pins
  - 35mm x 35mm x 4mm
  - 0.5mm pitch



RICH Detector – 'Mosaic' Assembly

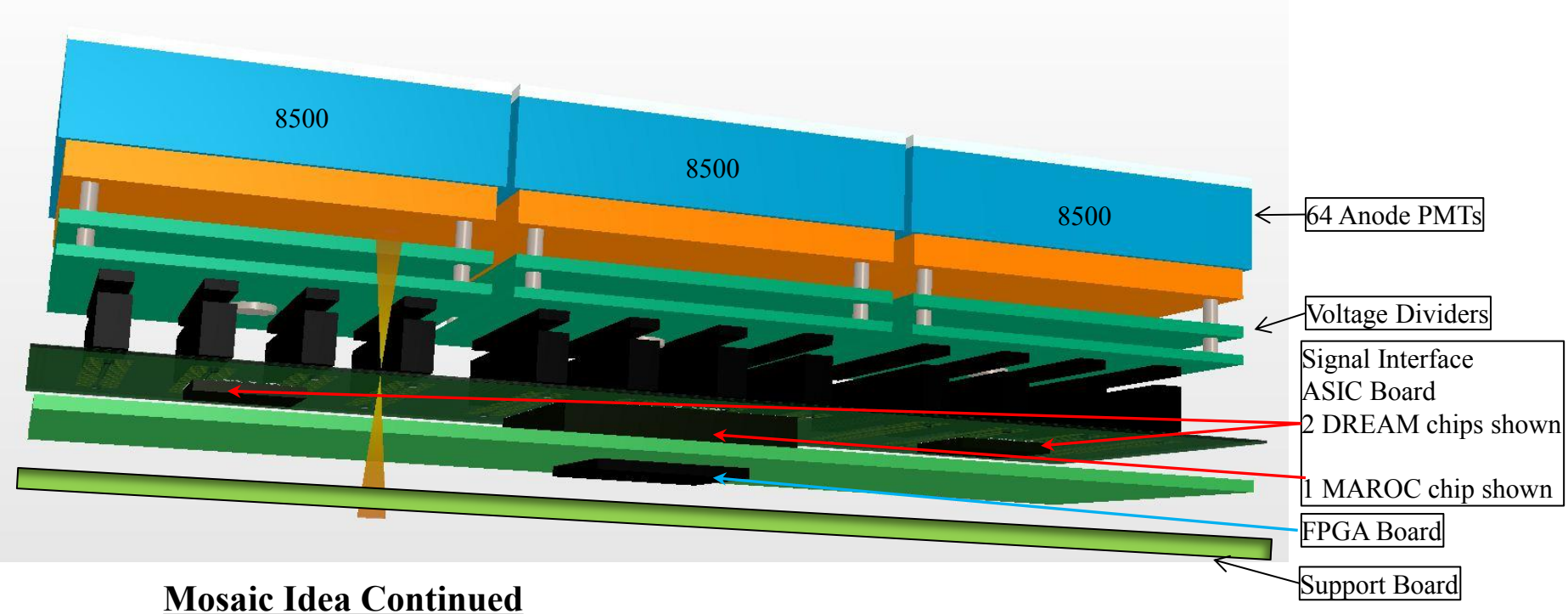


Side View

Mosaic Idea

- Design two 'Motherboards'
  1. Two 8500 tubes
  2. Three 8500 tubes (shown)
- Forty (40) of each Motherboard type
- One FPGA for each Motherboard supports I/O for ASIC chips
- Reduction of cabling
- Another board would support several "Mosaic" assemblies
  - Provides mechanical support
  - Low voltage distribution
  - HV bias for several "Mosaic" sections

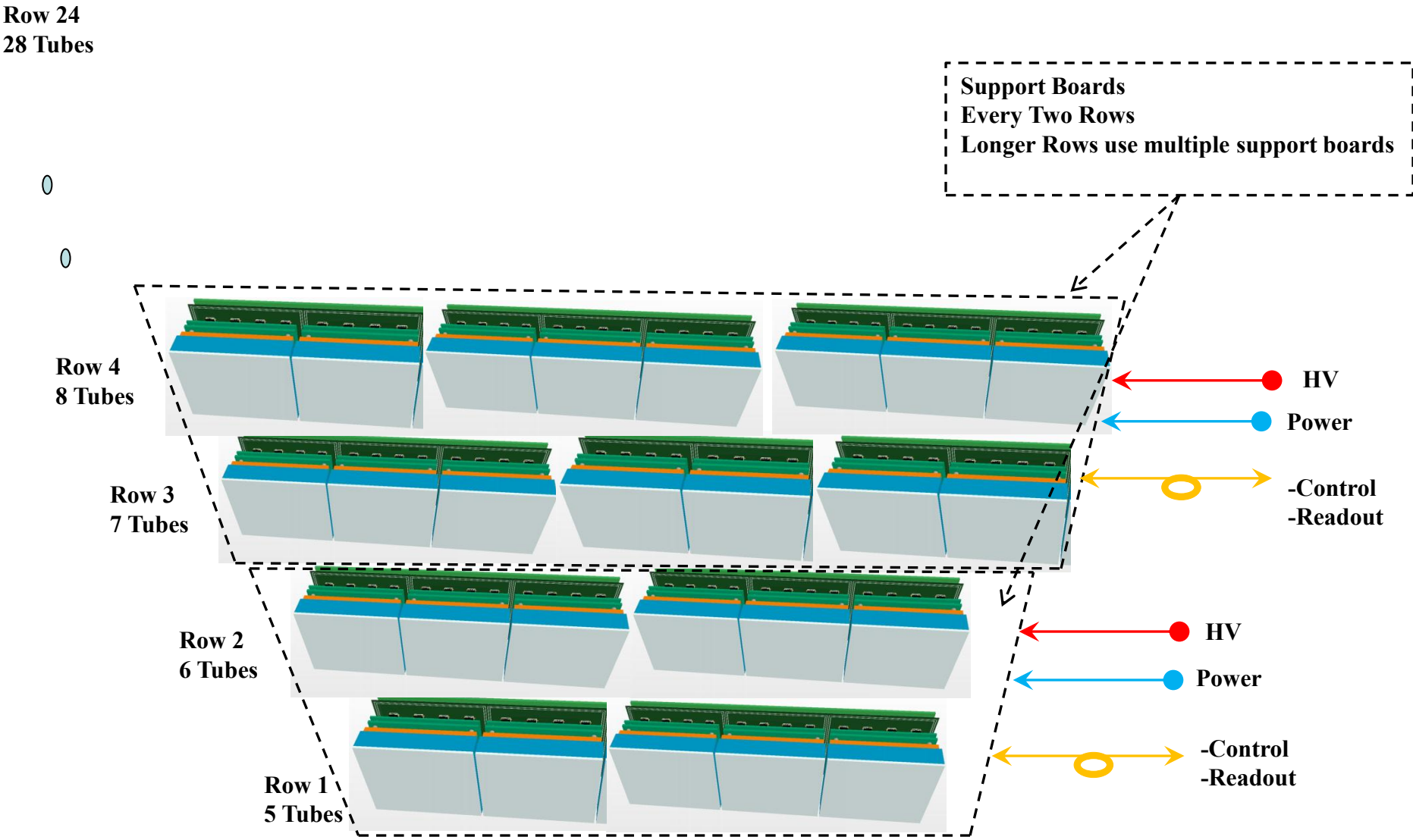
RICH Detector – 'Mosaic' Assembly



Mosaic Idea Continued

- Two ASICs shown for detail only
  - DREAM
  - MAROC3
- Reduction of cabling
- Support board services several "Mosaic" assemblies
  - Provides mechanical support
  - Low voltage distribution
  - HV bias for several "Mosaic" sections

RICH Detector – 'Mosaic' Assembly
(Rough Sketch)



Summary

Mosaic Idea

- Two 'Motherboard' designs only
  1. Two 8500 tubes
  2. Three 8500 tubes (shown)
- Forty (40) of each Motherboard type
- One FPGA for each Motherboard supports I/O for ASIC chips
- Significant reduction of cabling
- Support Board services several "Mosaic" assemblies
  - Provides mechanical support
  - Low voltage distribution
  - HV bias for several "Mosaic" sections
  - Few active components, low cost, DC or low speed signals

Action Items:

- Selection of FPGA needs to be analyzed
  - Need fairly high I/O pin count
  - FPGA must have serial link bandwidth to manage data from ASIC chips
- Cost analysis for circuit boards and cabling issues