CLAS12 Ring Imaging Cherenkov (RICH) Detector

Mid-term Review

Front End Electronics

INFN - Ferrara

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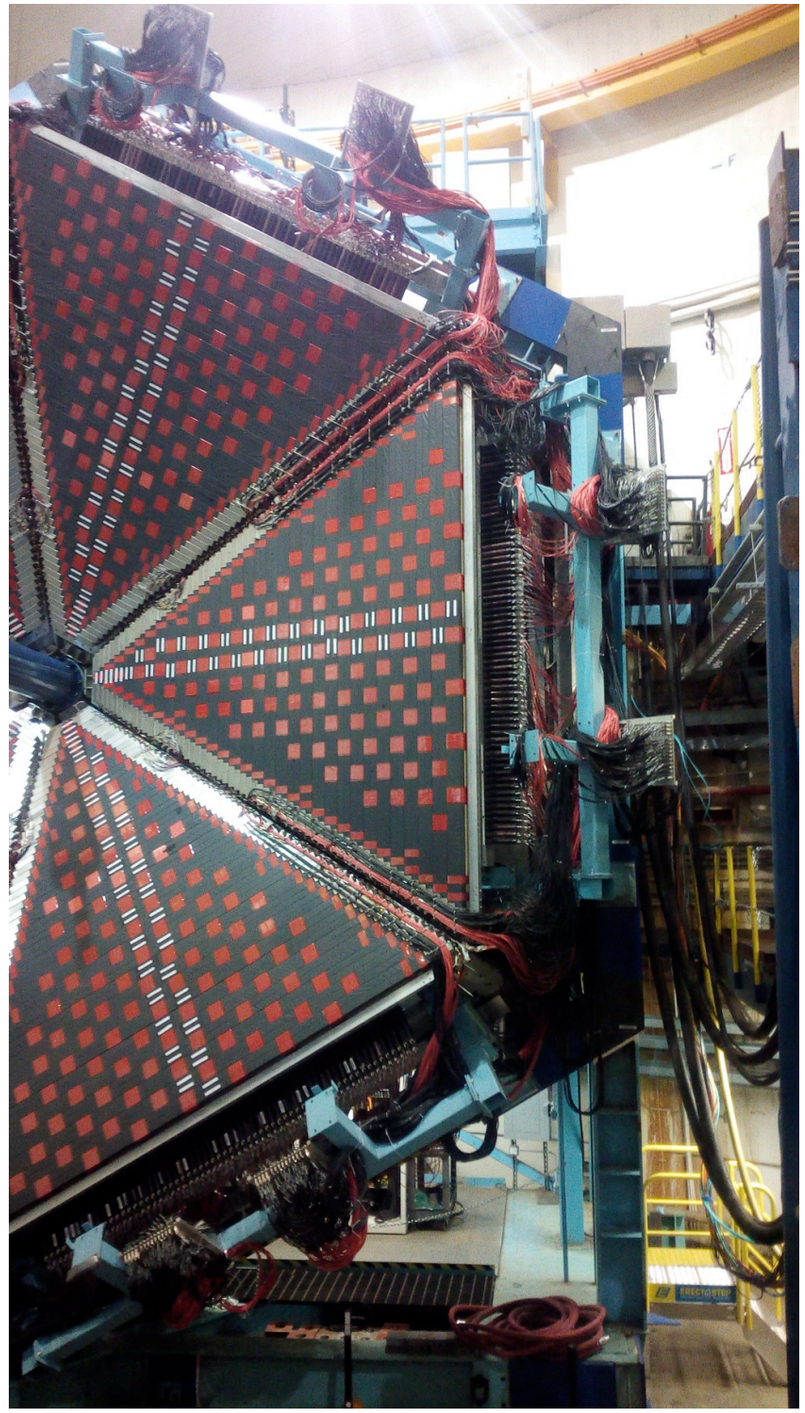
Overview

- Readout requirements
- Hardware design
- Electronics boards
- Integration in CLAS12
- Services
- Status

RICH READOUT requirements

1 m^2 of single photoelectron sensitive surface (25000 channels)

- 100% efficiency at 1/3 photoelectron (50fC)
- Gain spread compensation 1:4
- Time resolution 1 ns
- Trigger rate 20kHz
- Latency 8 μs
- Radiation tolerance adequate for CLAS12



Front End chip

Multi Anode Read Out Chip (**MAROC**) is a 64 channel Application Specific Integrated Circuit (ASIC) fabricated in AMS SiGe 0.35 µm technology.

MAROC is expected to discriminate the 64 channels PMT output signals and produce 64 corresponding **binary outputs.** The charge measurement is also available.

The ASIC is configured, controlled and readout by an FPGA

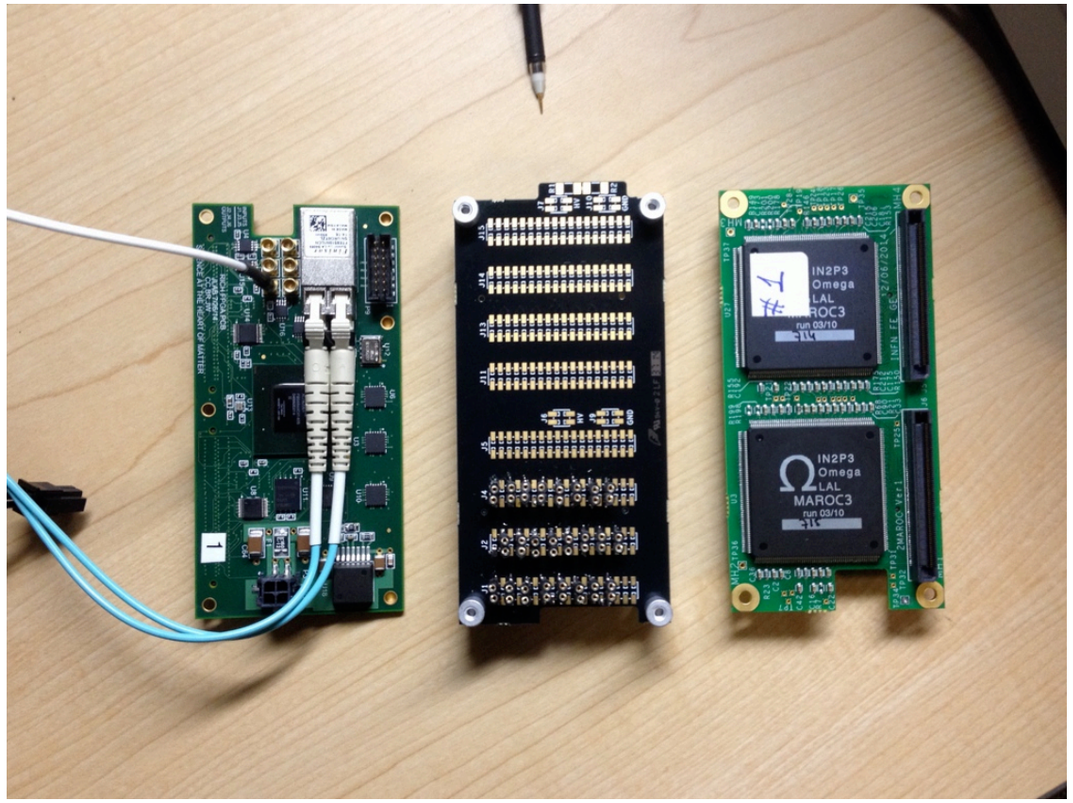
- Single Channel preamplifier with adjustable gain (1:4)
- Highly configurable shaping section
- Binary outputs come from a **fast shaper** followed by a **discriminator.** Threshold is set by a 10 bit DAC
- Two Track and Hold provide a multiplexed charge output. A digital version of this measurement is also embedded in the chip

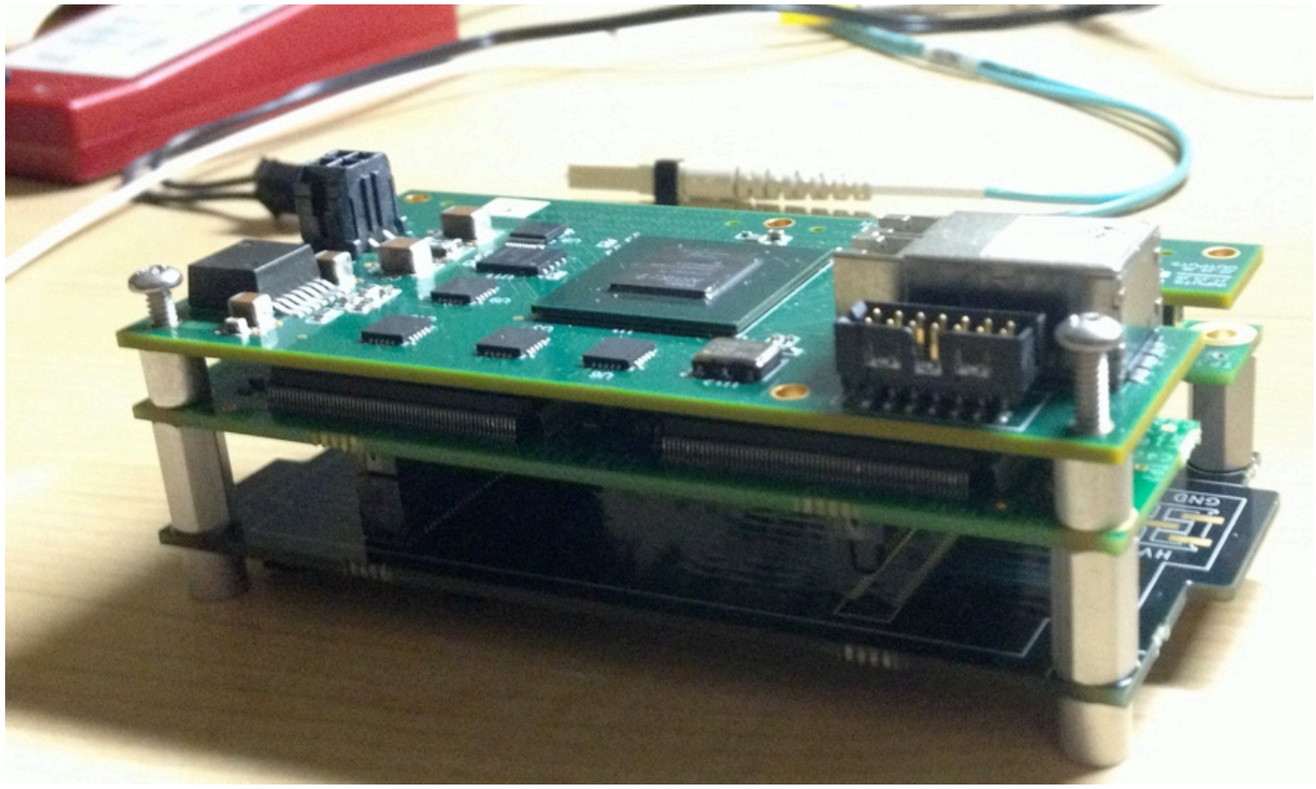
Multi **A**node- **R**ead **O**ut **C**hip
version 3
64 Channel
1.5 mW/channel
by Omega Group
Application Specific
Integrated Circuit (ASIC)

64 channels parallel binary outputs introduces negligible dead time

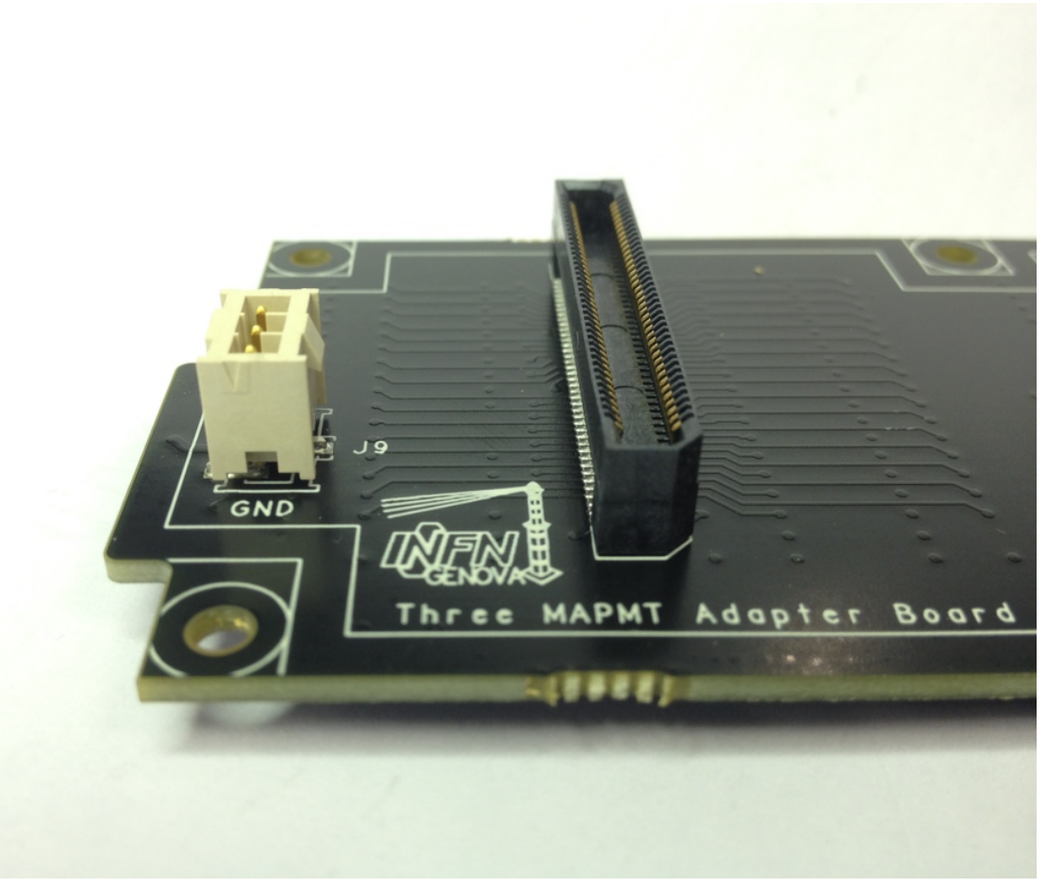
RICH MAPMT Assembly

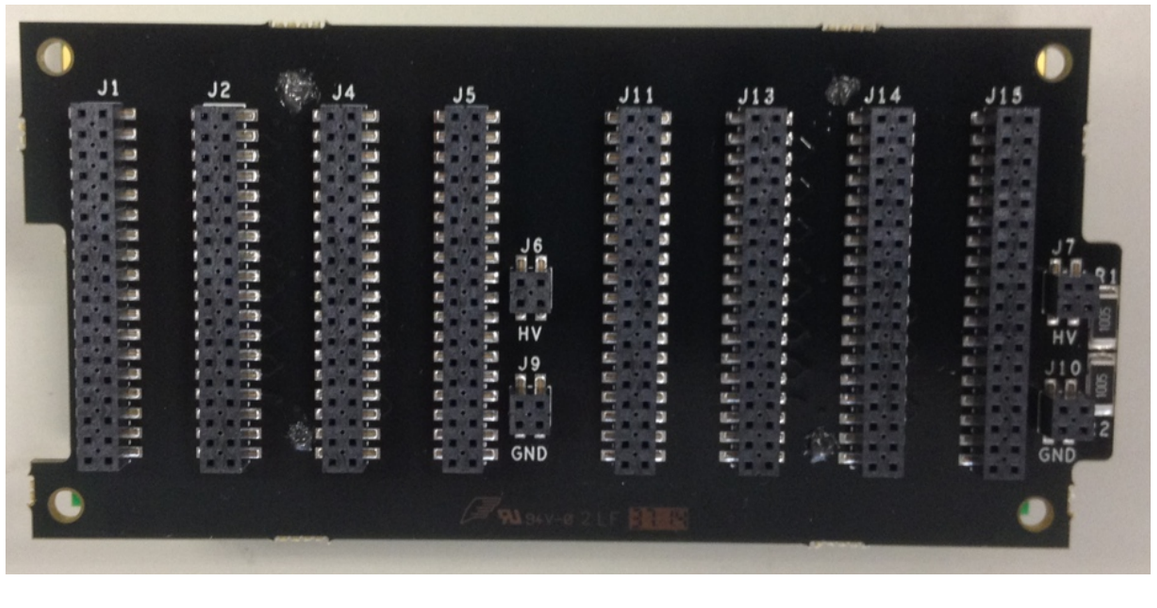
- The CLAS12 RICH detector will use compact front end unit (Tile) to readout the MAPMTs
- A tile is composed by three boards: MAPMTs Adapter, ASIC board and FPGA board
- Complete tessellation of the electronics panel requires 2 variants:
  - 2 MAPMT/2 MAROC/128 pixel (100 mm x 50 mm)
  - 3 MAPMT/3 MAROC/192 pixel (150 mm x 50 mm)
- Four prototypes have been produced in October 2014





ADAPTER board

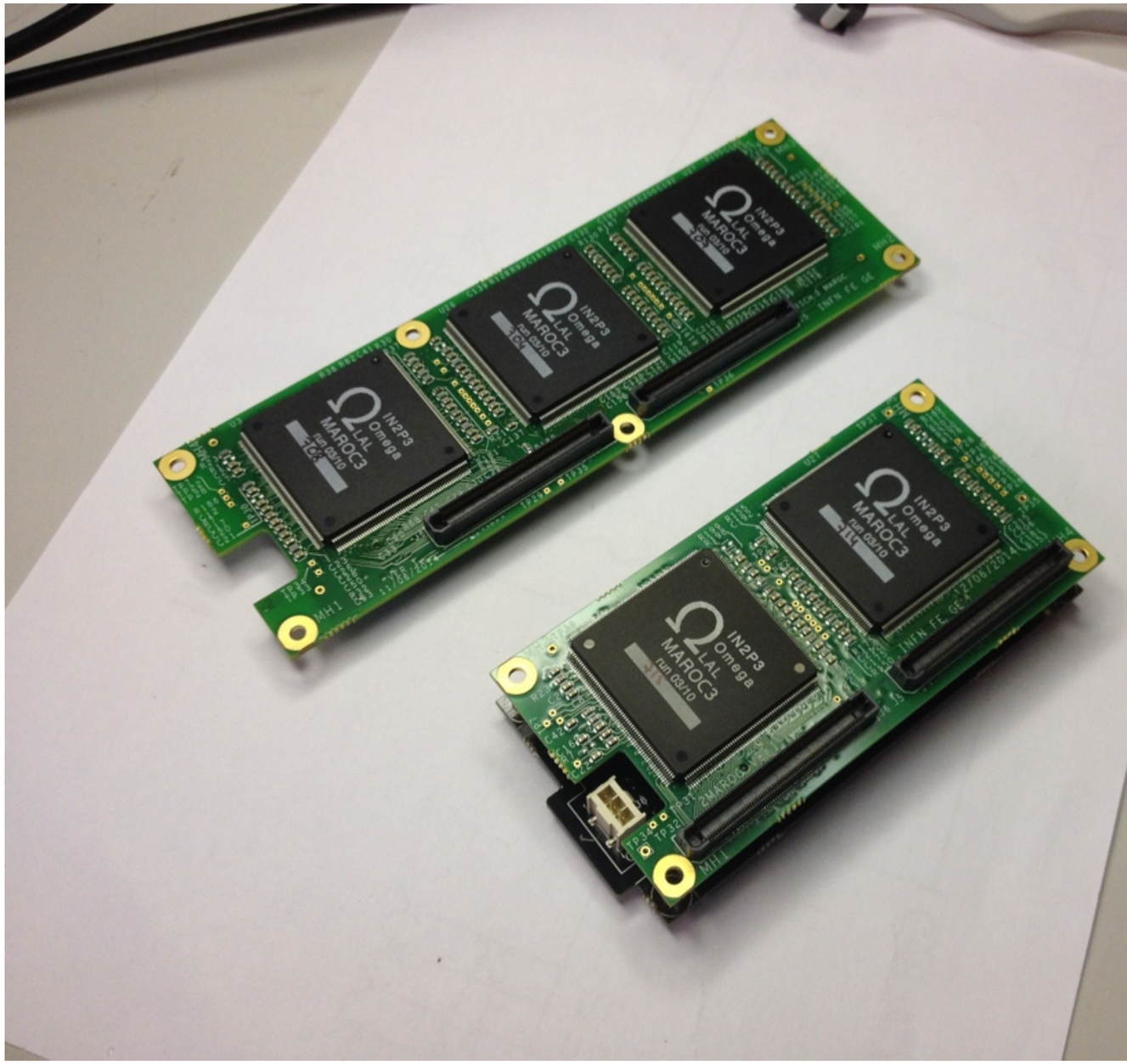




- Passive board
- Light Tight
- Provides HV power to the PMTs and low capacitance electrical connectivity with MAROC
- 16 prototype produced (8 per variant)
- Mechanical, electrical and light tighness tests completed
- 2 boards modified to be used as charge injection board during characterization phase

ASIC board

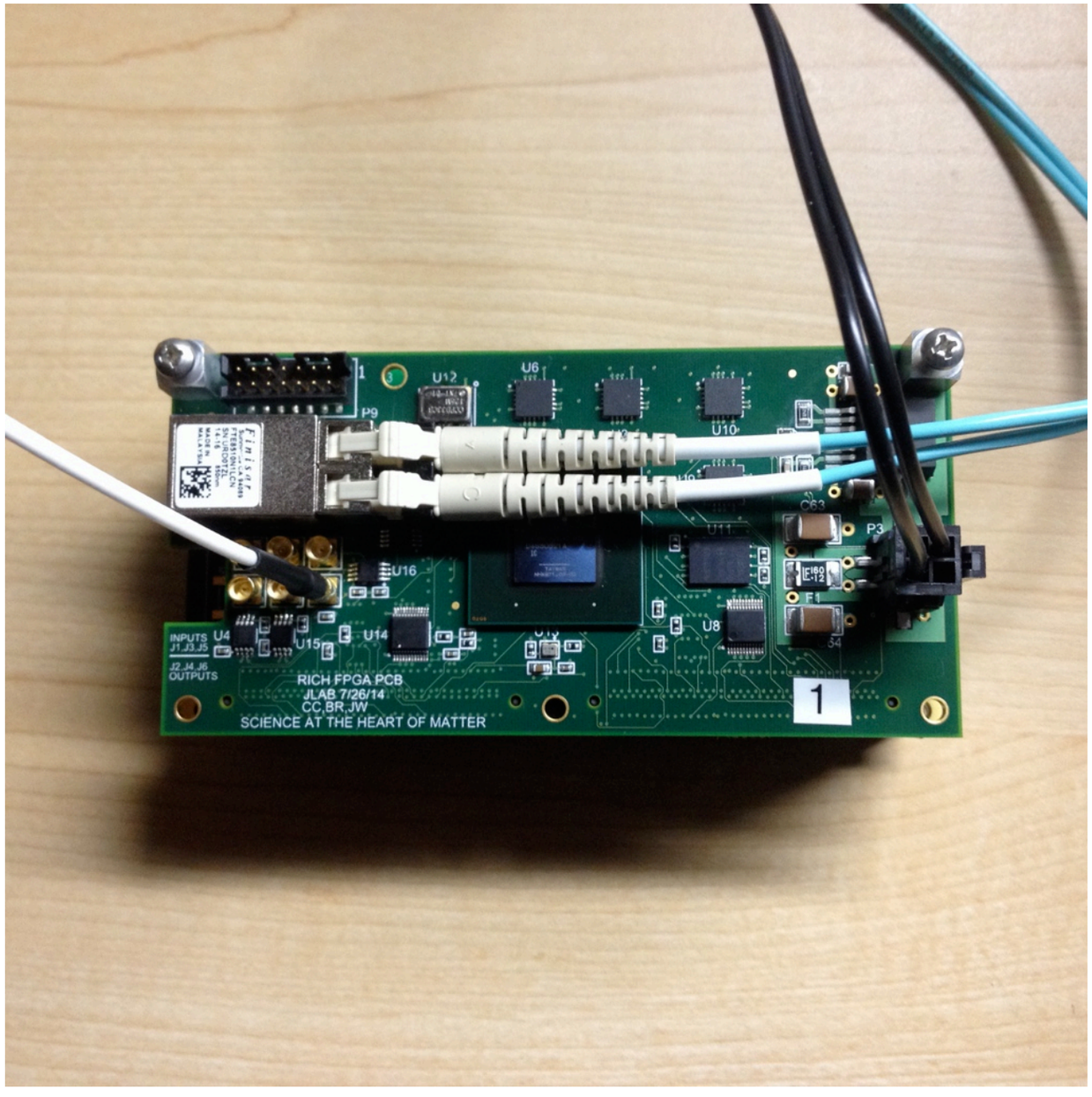
- Houses the MAROC, Voltage regulator, Test Pulse circuit, External ADC
- Provides interface with MAPMT and FPGA
- 2 versions 192 or 128 channels
- 4 ASIC boards available since October 2014
- Internal pulser revised in June 2015



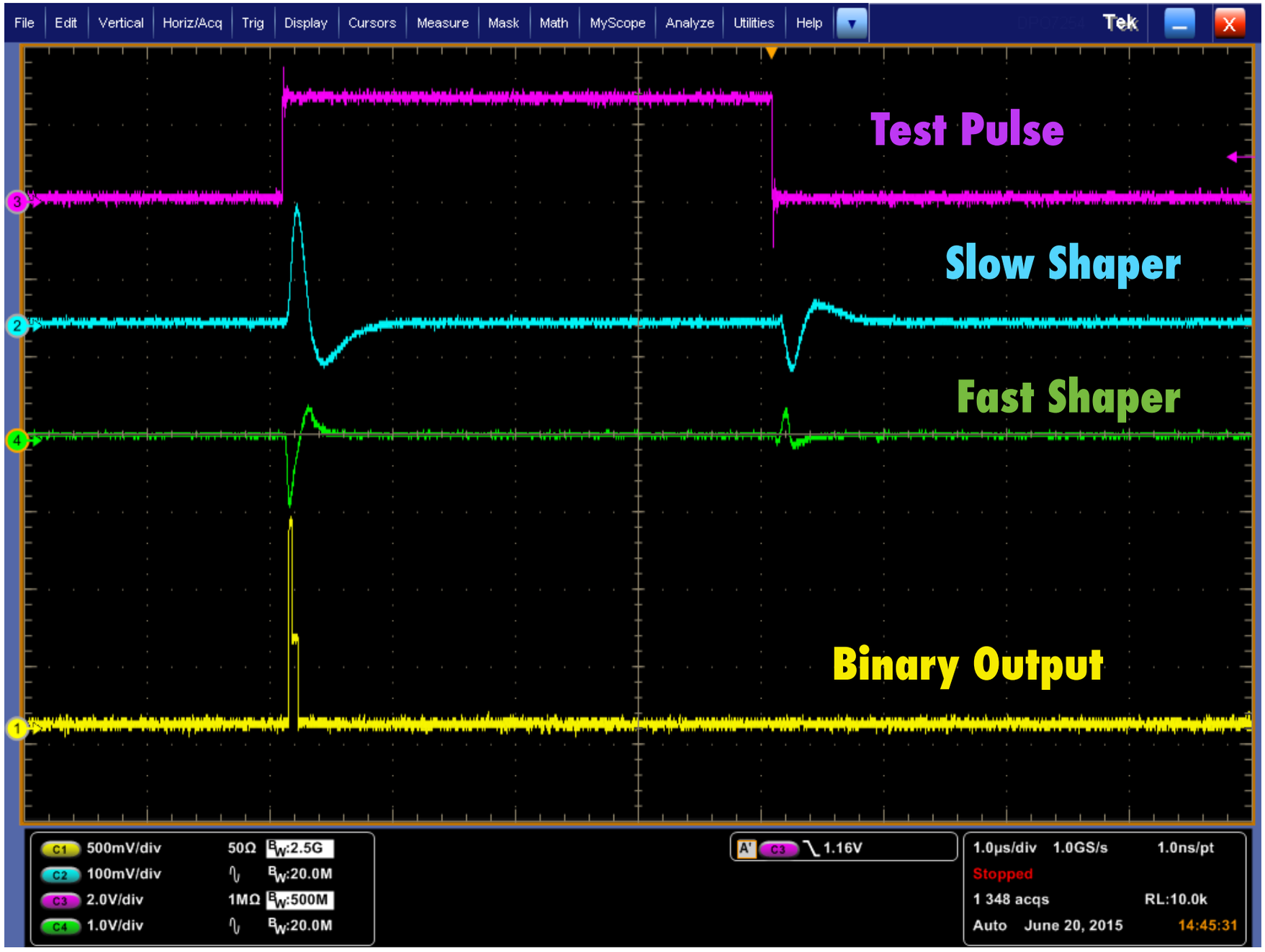
- Electrical tests passed
- Slow Control completed
- Characterization completed
- TDC readout completed
- ADC readout in progress

FPGA board

- FPGA board provides the following features:
  - Support 2 or 3 MAPMT/MAROC
  - 192 channels of 1 ns resolution TDC
  - Single fiber optic interface: TDC reference clock, fixed latency trigger, MAROC slow controls, stream triggered data to event builder
- Low power (3 MAROC + FPGA + optical transceiver): 3.8W for 192 channels
- Interfaces directly to PC over ethernet (1Gbit) for small setups

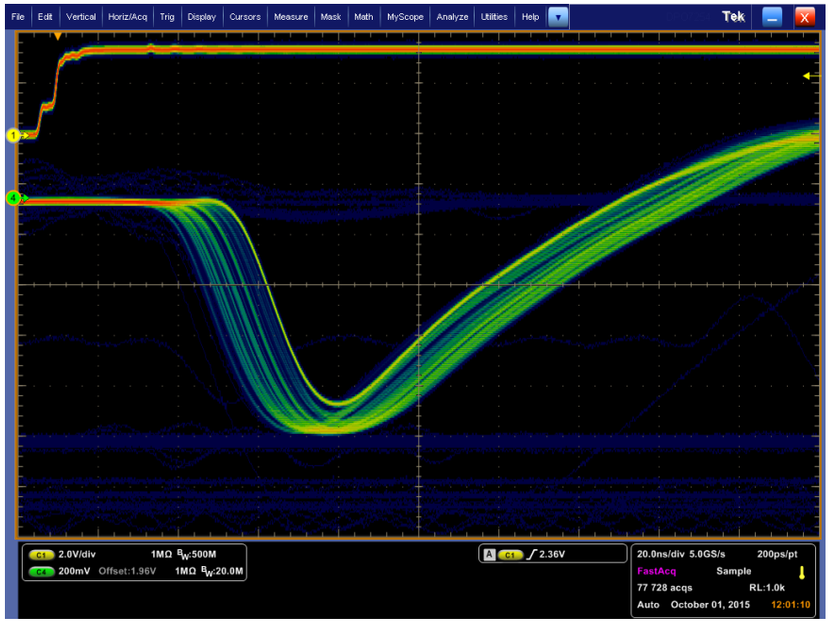


MAROC analog response



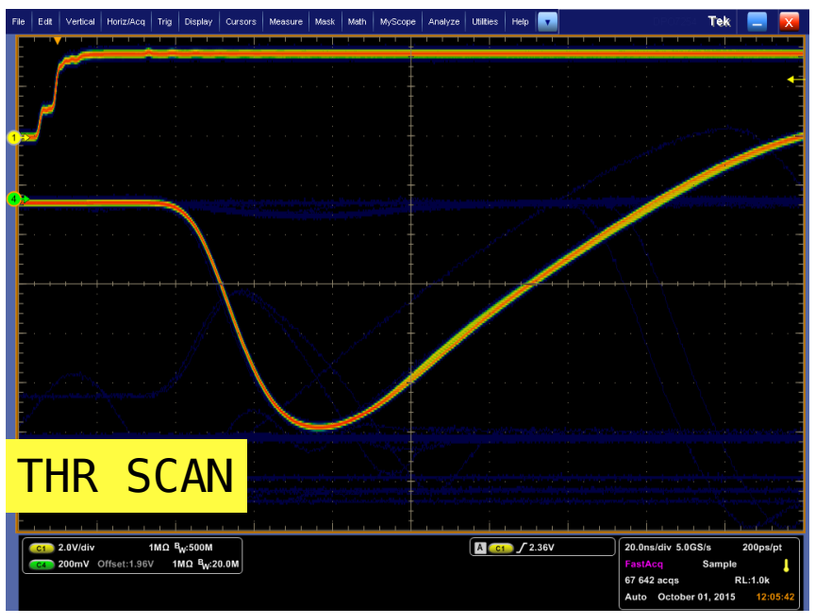
- Single Channel complete test pulse response.
- Charge level 4–5 photoelectrons
- The weak response to positive charge (due to falling trailing edge of the step function) can be eliminate with proper threshold setting

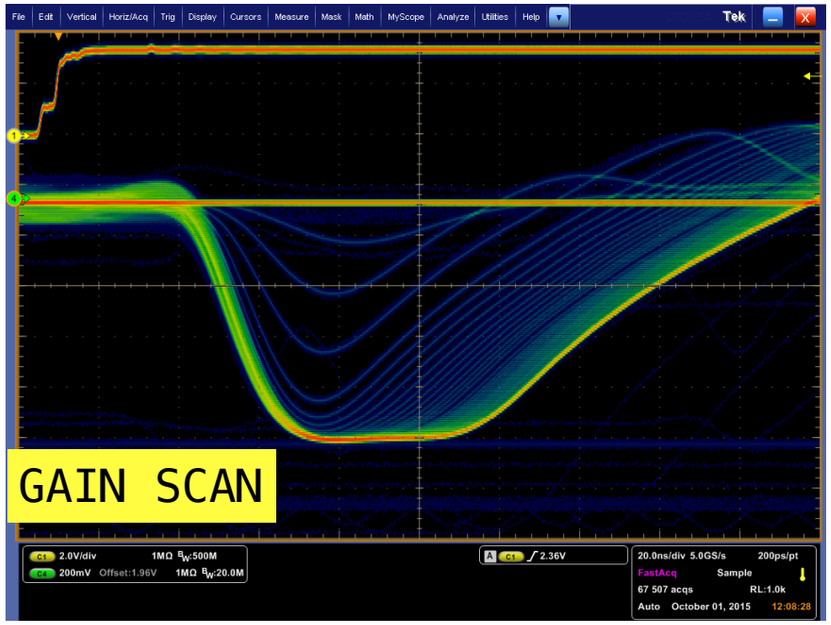
MAROC Fast Shaper response



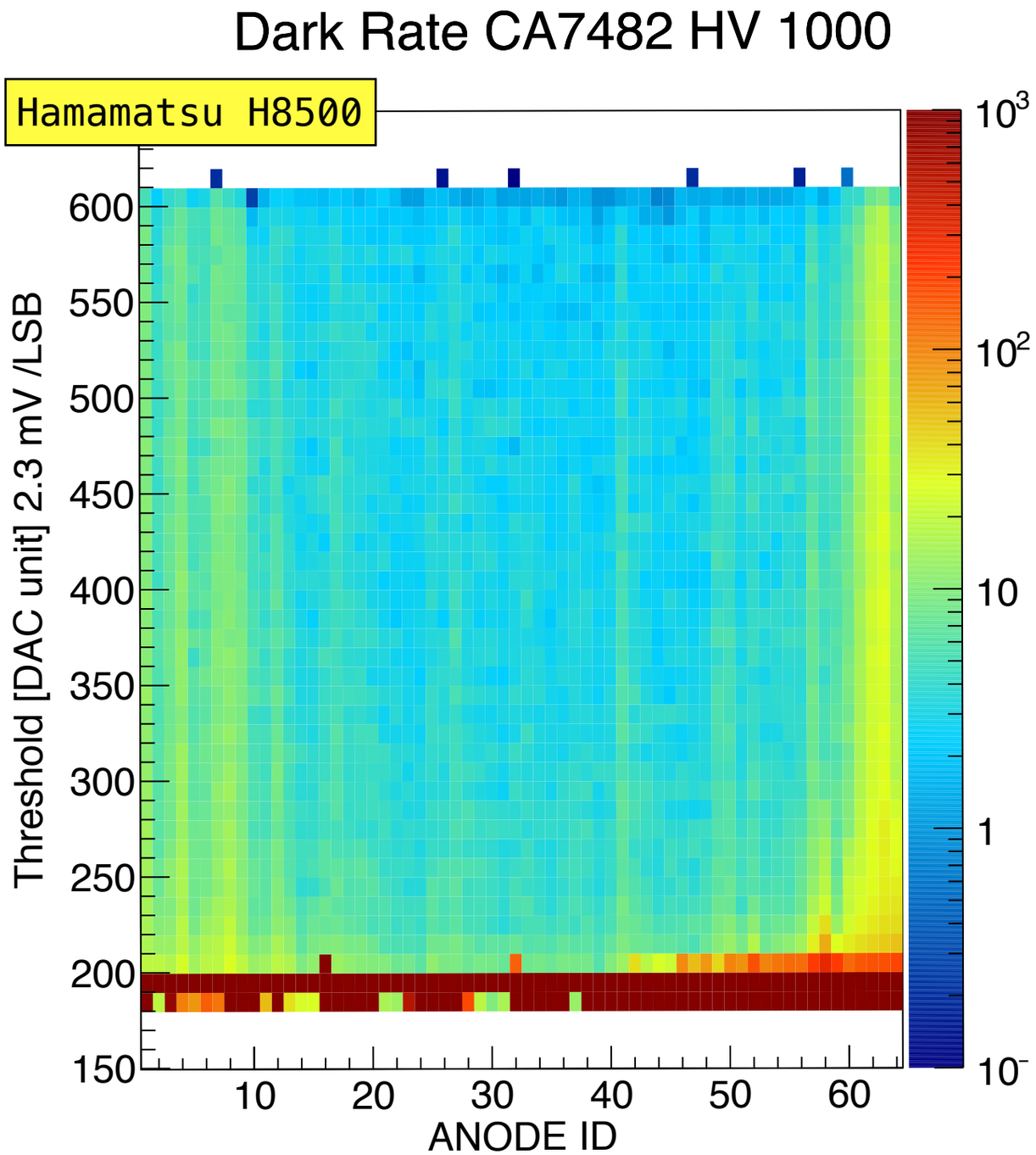
64 channel fast shaper response

Single channel





Dark Rate Test



Scaler measurements (August 2015, Jlab)

Rate compatible with datasheet

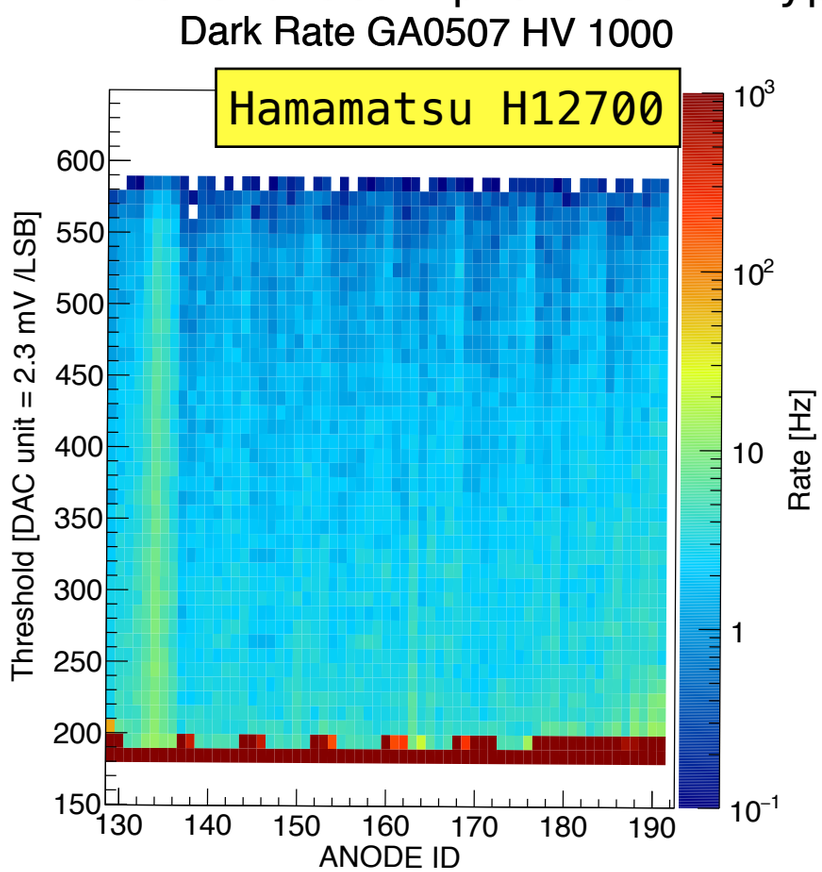
(1kHz per MAPMT)

Single channel dark rate

Photocathode uniformity

HV and Gain scanned

Threshold scan plot for 2 type of MAPMT



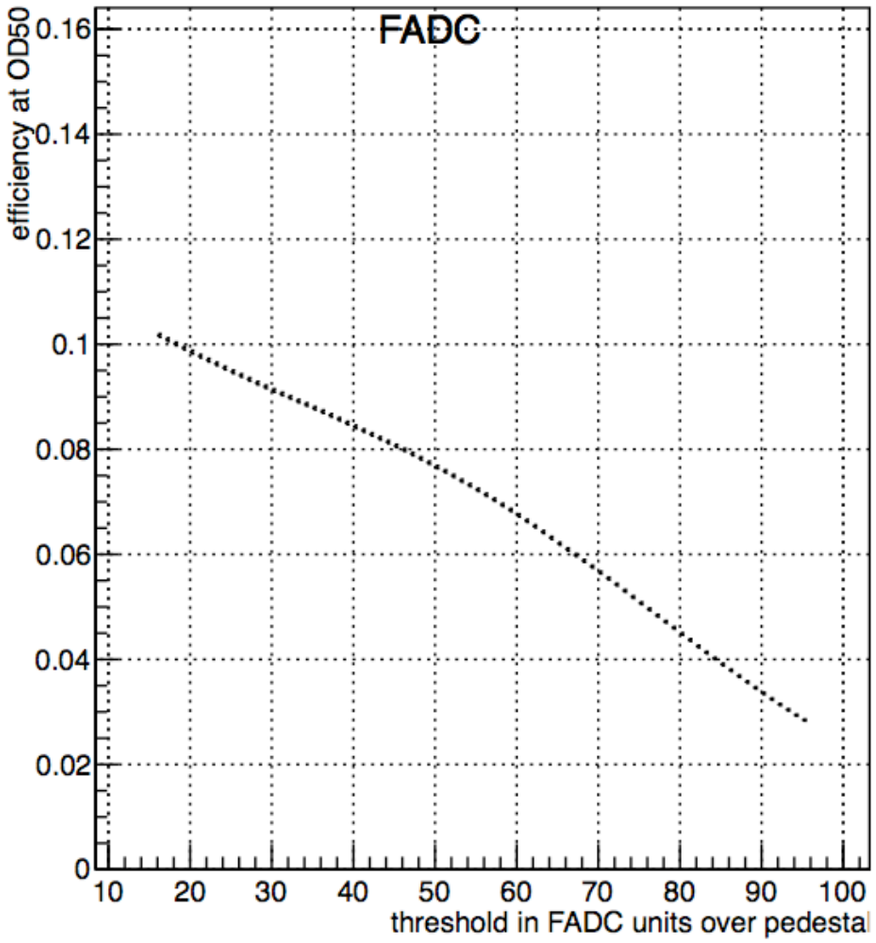
Laser Efficiency Test

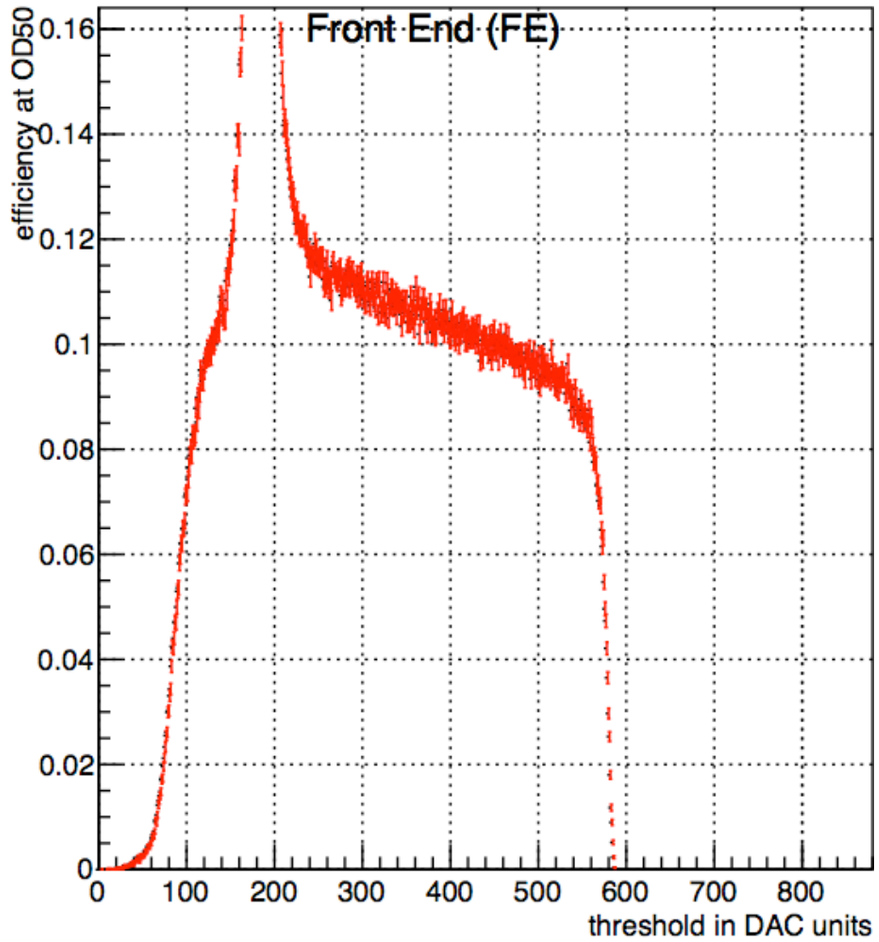
Scaler measurements (August 2015, Jlab) HV and preamp Gain scanned at different Light intensity

Plots show fADC (baseline equipment at JLab) and MAROC counting efficiency in the same conditions against the threshold in the corresponding systems.

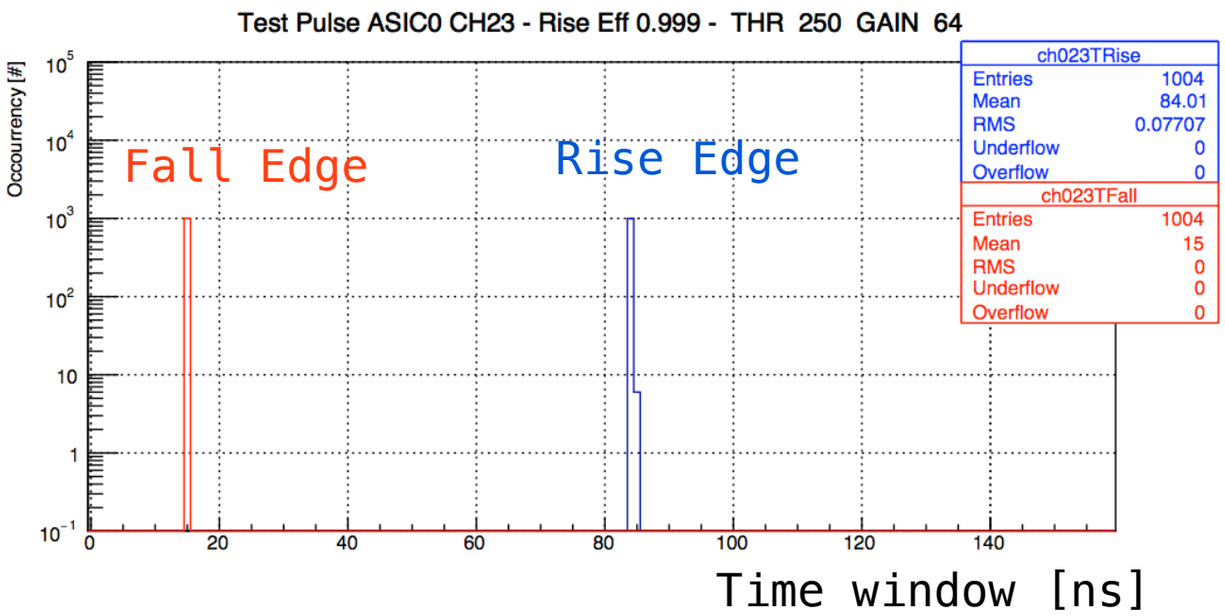
MAROC performs slightly better than fADC

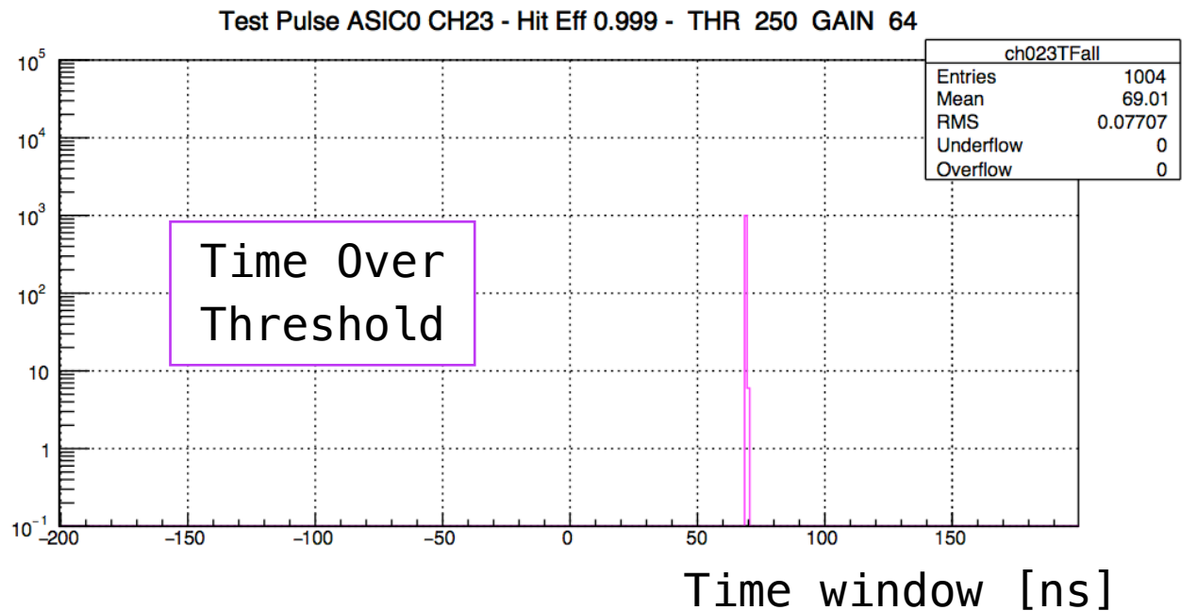
Efficiency = #hit/#total events



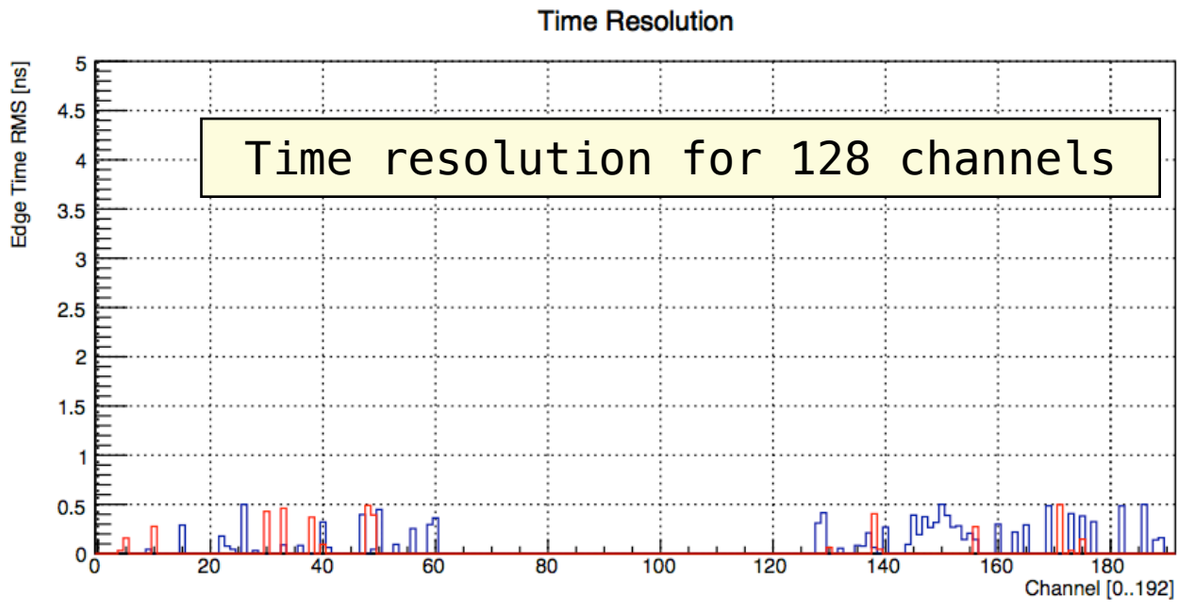


Time Resolution





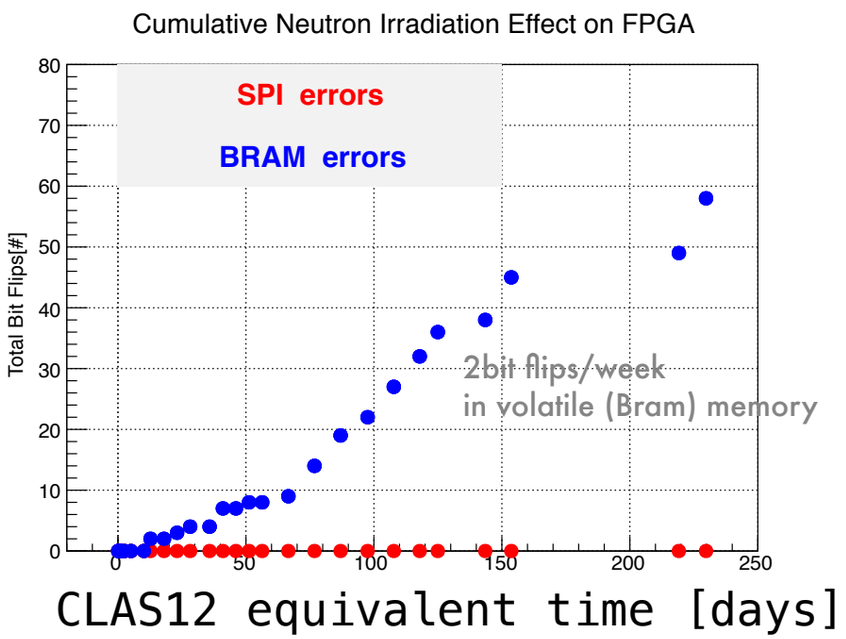
- Test Pulse TDC response
- Time resolution below TDC sensitivity (1ns)
- Good Uniformity
- Time over Threshold study in progress

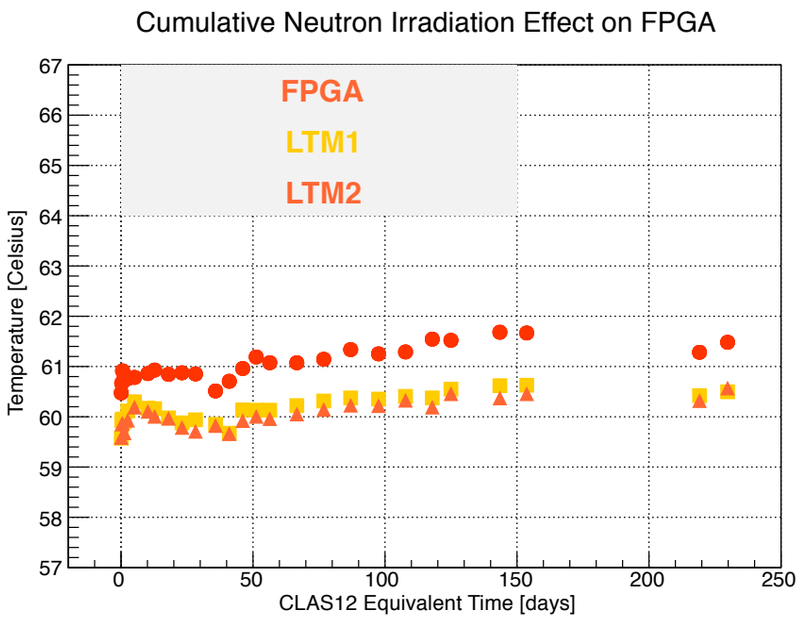


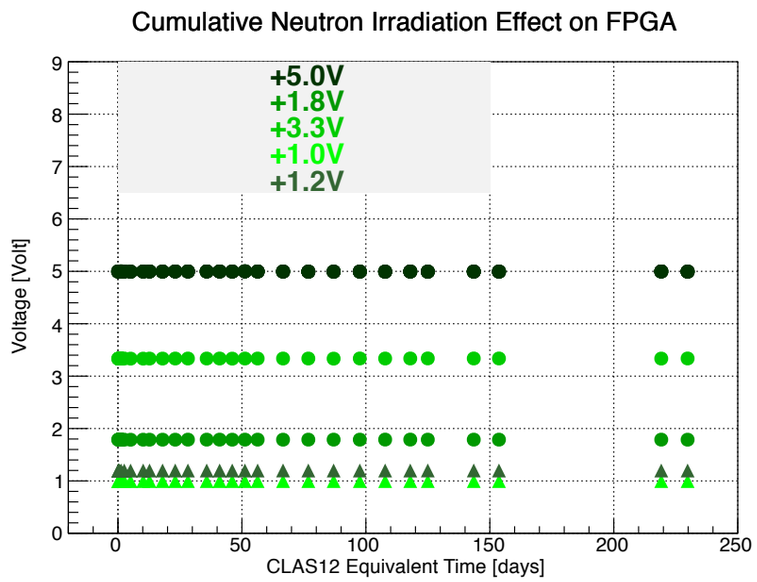
Channel [0..192]

Radiation Tolerance Test

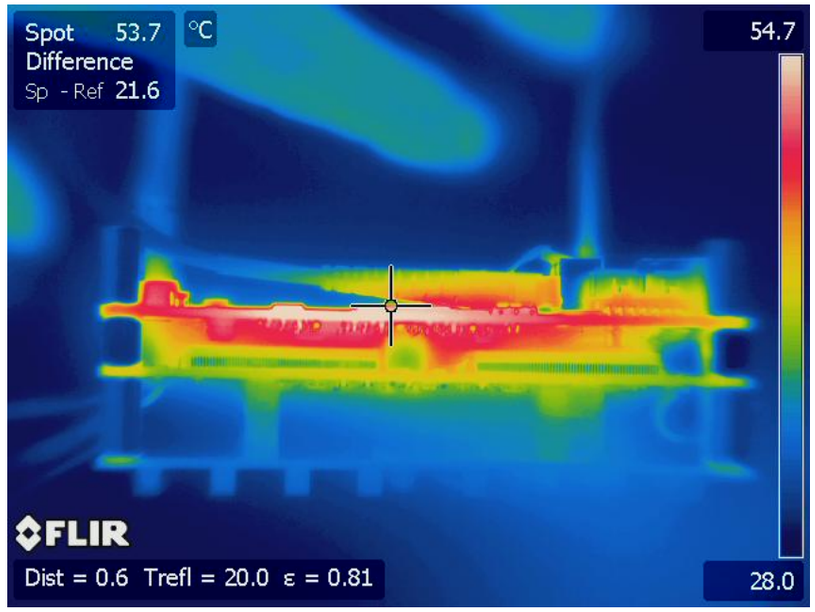
- Xilinx Artix7 FPGA and Finisar Endurance optical transceiver are new products and poor data are available about their radiation tolerance.
- A first irradiation test with neutrons at Frascati Neutron Generator (FNG, Italy) has been performed October 2015. Other test are planned in November 2015
- Bit flips in FPGA, Transceiver/Voltage regulators/Temperature anomalies monitored online using the same optical fiber link.
- Equivalent CLAS12 dose 8 months at full luminosity so far analised
- Zero errors on static memory (the firmware image is not corrupted)
- Few errors on volatile memory (Bram), easy to recover
- Plots show Bit Flips, Temperature and Voltage. Analysis is ongoing.

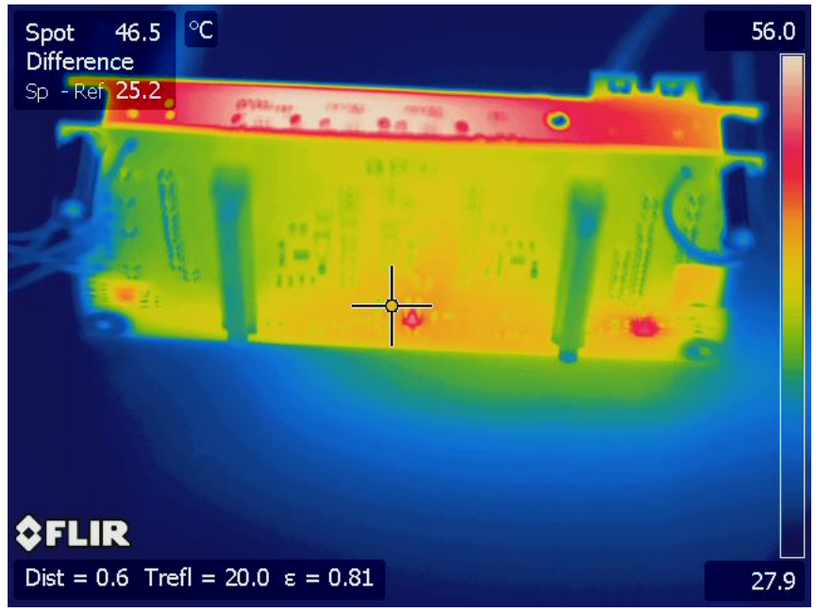


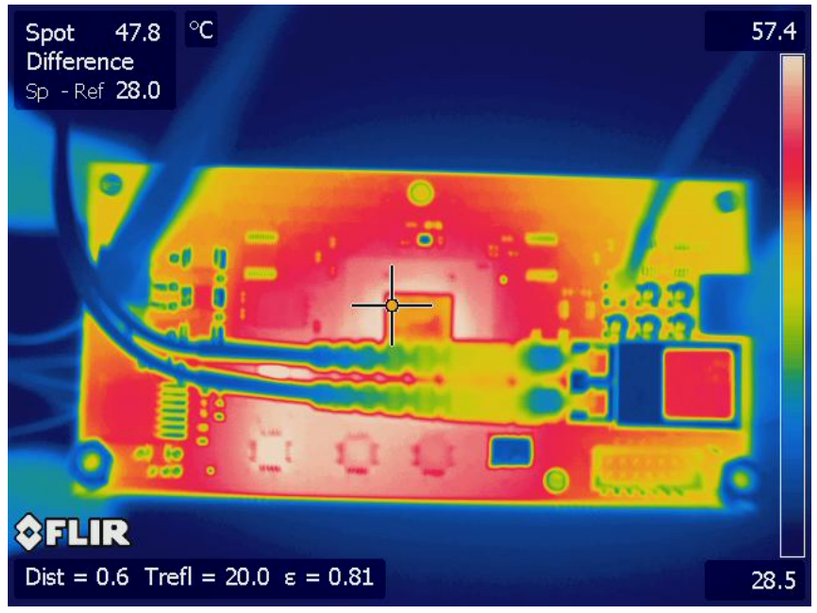




Heat Production







Thermografic camera images shows distribution of heat production in the tile.

Fpga,optical transceiver and voltage regulator are the main sources of heat production

- Power Consumption @ 5Volt:

  760 mA (3.80 Watts) 3ASIC variant (x115)

  670 mA (3.35 Watts) 2ASIC variant (x23)
- Total power: 514 Watts

Acceptance Test

Level 0: electrical test and power dissipation (manual)

Level 1: automatic diagnostic (c++ library and bash script completed in Sept 2015)

1. 64 channels input + test channel pin
2. Slow Control check (gain,shaping,threshold, masked OR)
3. Binary outputs 100% efficiency at 50 fC (1/3 photoelectons)
4. Time resolution (1 ns)
5. Charge response in range 10fC..1000fC

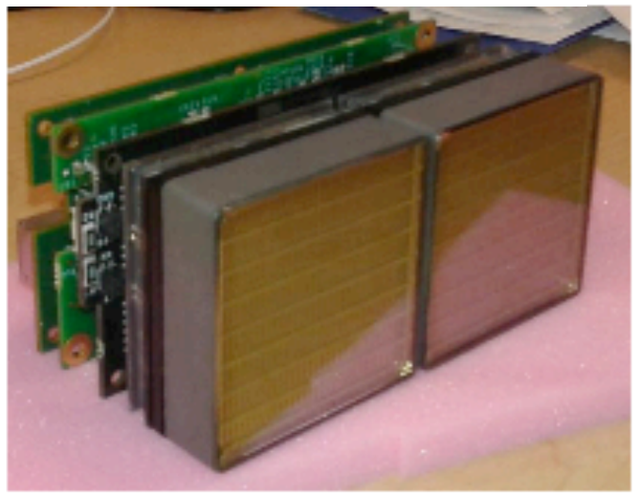
Hardware Requirements: FPGA board, Injection Board, External Pulse generator

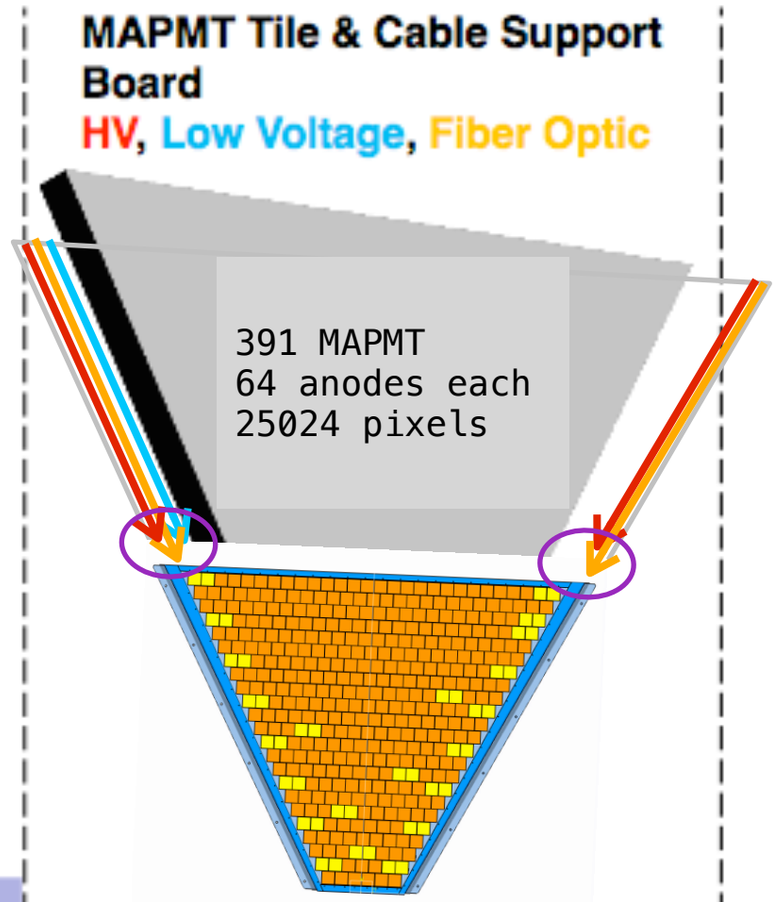
NOTE1: Preamp gain = 0 allows muting unwanted channels

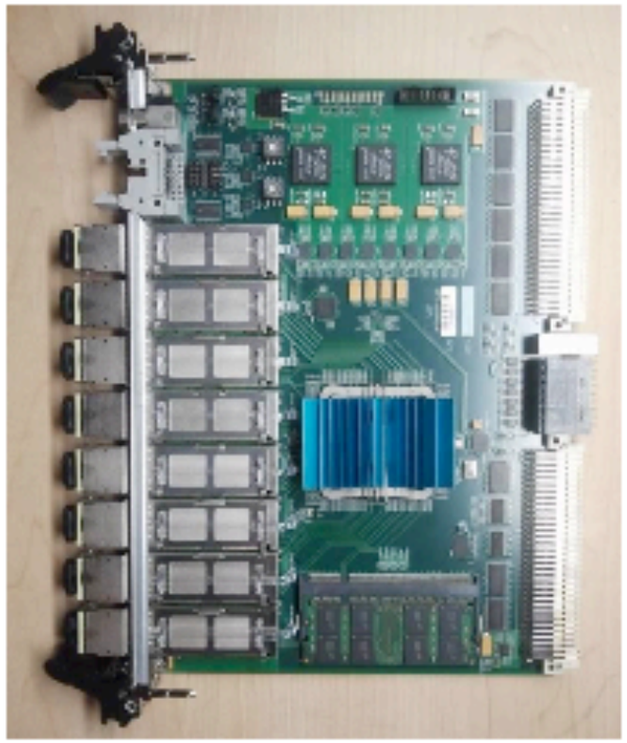
NOTE2: External pulser driven by FPGA board for synchronization

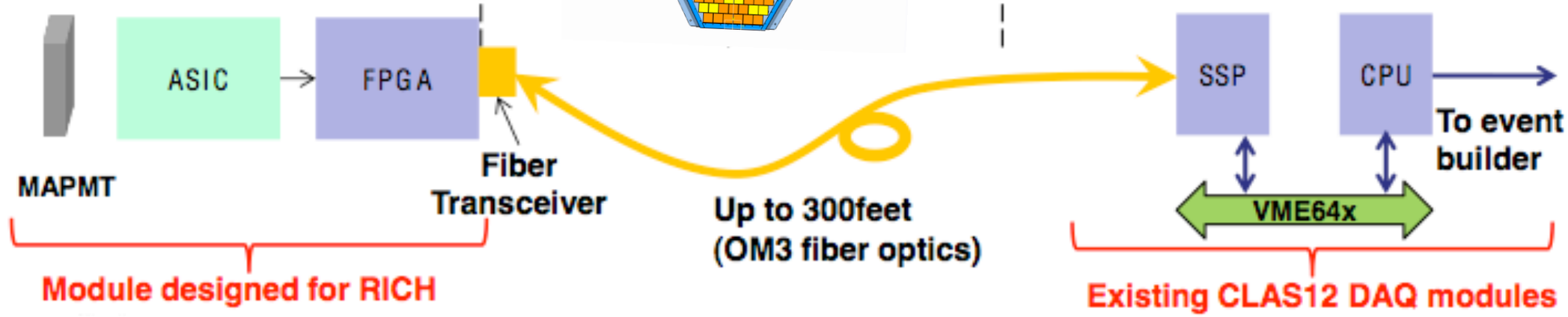
RICH DAQ in CLAS12

MAPMT “Tiles”
Two Tile Types:
2MAPMT per Tile
OR 3MAPMT per Tile
(138 Tiles per sector)
391 TOTAL MAPMT

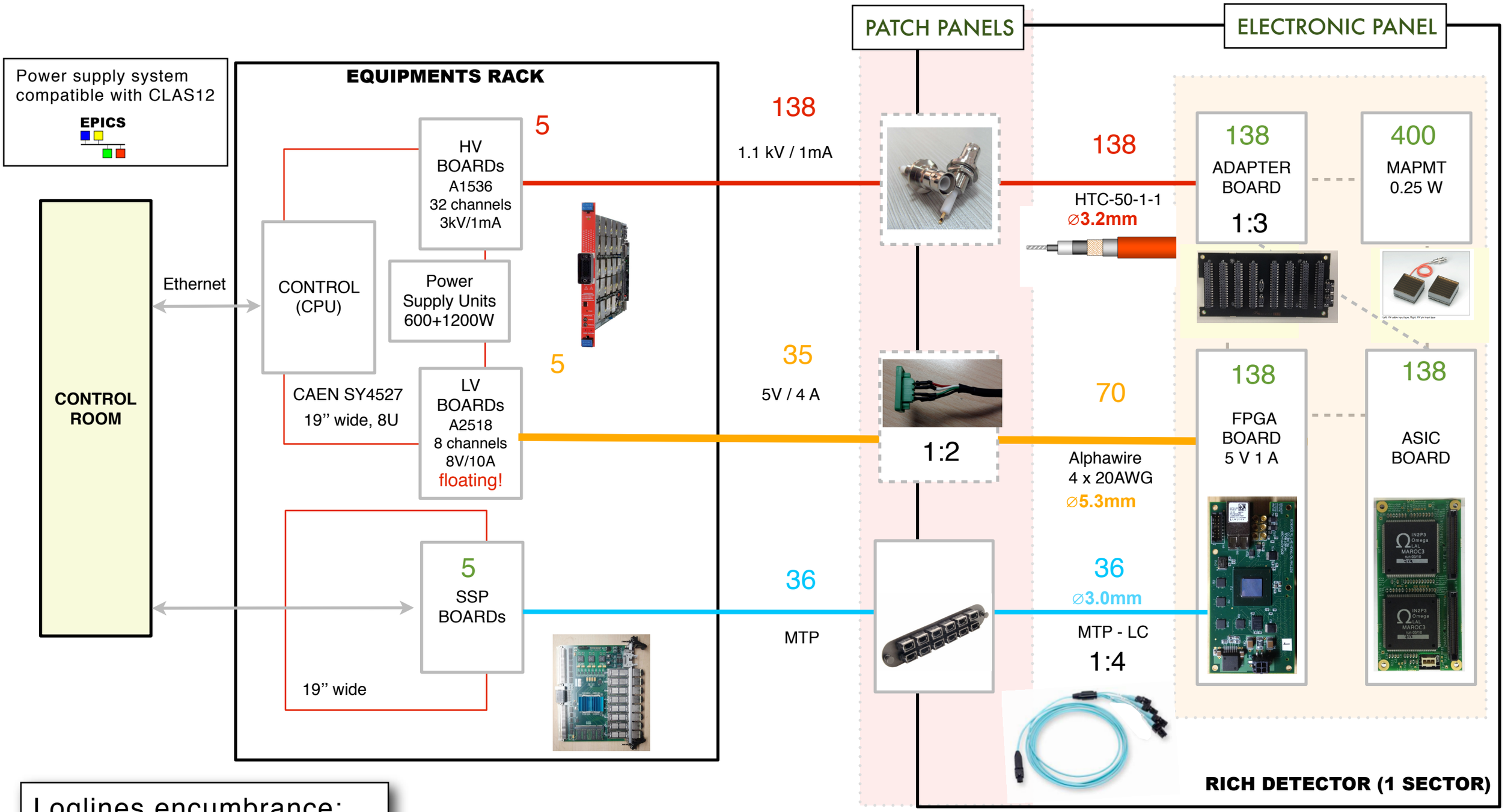








Service scheme diagram



Loglines encumbrance:
High Voltage - 1413 mm²
Low Voltage - 1966 mm²
Optical Fiber - 324 mm²
TOTAL = 3704 mm²

Conclusions

- Design completed
- Prototype produced and tested
- TDC satisfy the requirements (Physics Run & Calibration protocol)
- ADC part in progress (Debug protocol)
- Tiles satisfy all the requirements
- Production ongoing