CLAS12 Ring Imaging Cherenkov (RICH) Detector

Mid-term Review

Front End Electronics

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2015 October 13th

Overview

- Readout requirements

- Hardware design

- Electronics boards

- Integration in CLAS12

- Services

- Status

- Plan

RICH READOUT requirements

1 m^2 of single photoelectron sensitive surface (25000 channels)

- 100% efficiency at 1/3 photoelectron

- Gain spread compensation 1:4

- Time resolution 1 ns

- Trigger rate 20kHz

- Latency 8 μs

- Radiation tolerance adequate to CLAS12 environment
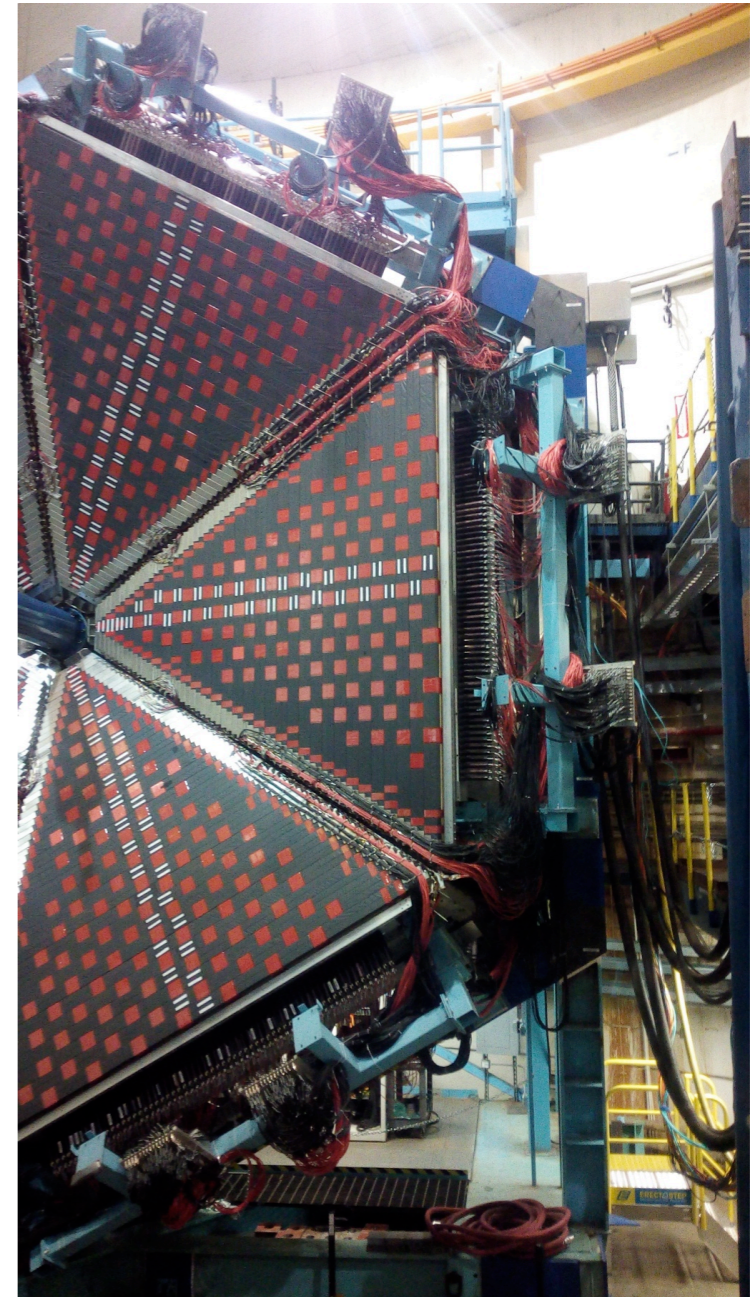
Front End chip

Multi Anode Read Out Chip (MAROC) is a 64 channel Application Specific Integrated Circuit (ASIC)fabricated in AMS SiGe 0.35 μm technology.

MAROC is expected to discriminate the 64 channels PMT output signals and produce 64 corresponding binary outputs. The charge measurement is also available.

The ASIC is configured, controlled and read out by an FPGA

- Single Channel preamplifier with adjustable gain (1:4)

- Highly configurable shaping section

- Binary outputs come from a fast shaper followed by a discriminator. Threshold is set by a 10 bit DAC

- Variable slow shaper (50–150 ns) followed by two Track and Hold provide a multiplexed charge output. A digital version of this measurement is also available by a 12 bit Wilkinson ADC

Multi Anode- Read Out Chip
version 3
64 Channel
3.5 mW/channel
by Omega Group
Application Specific
Integrated Circuit (ASIC)
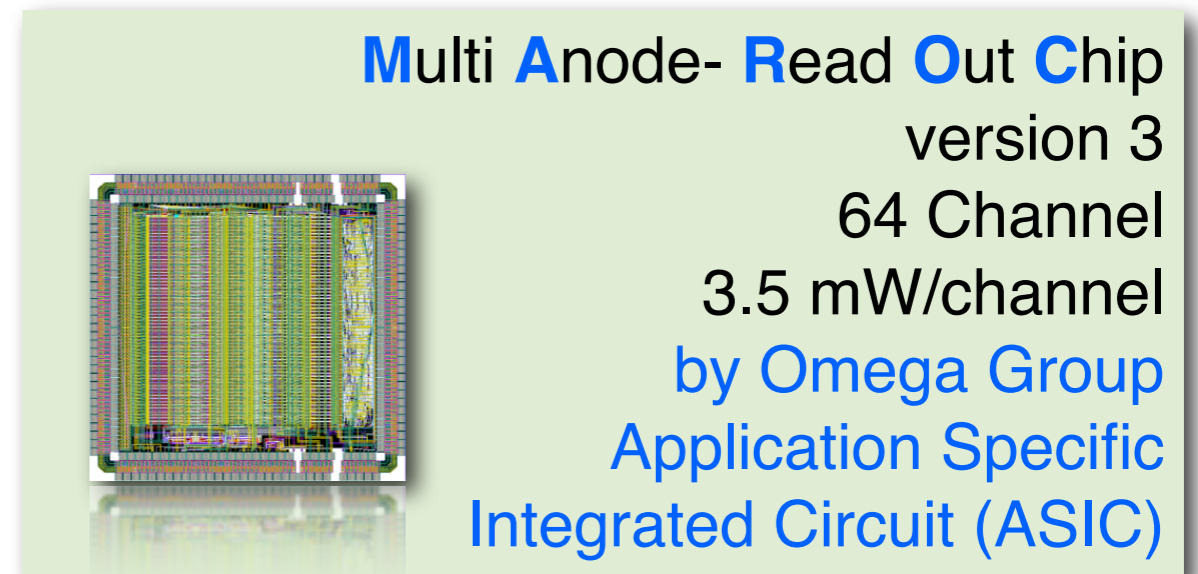
RICH MAPMT Assembly

- The CLAS12 RICH detector will use compact front end unit (Tile) to readout the MAPMTs

- A tile is composed by three boards: MAPMTsAdapter, ASIC board and FPGA board

- Complete tessellation of the electronics panel requires 2 variant:

  - 2 MAPMT/2 MAROC/128 pixel (100 mm x 50 mm) 700mA @ 5Volt

  - 3 MAPMT/3 MAROC/192 pixel (150 mm x 50 mm) 800mA @ 5Volt

- Four prototypes have been produced in October 2014
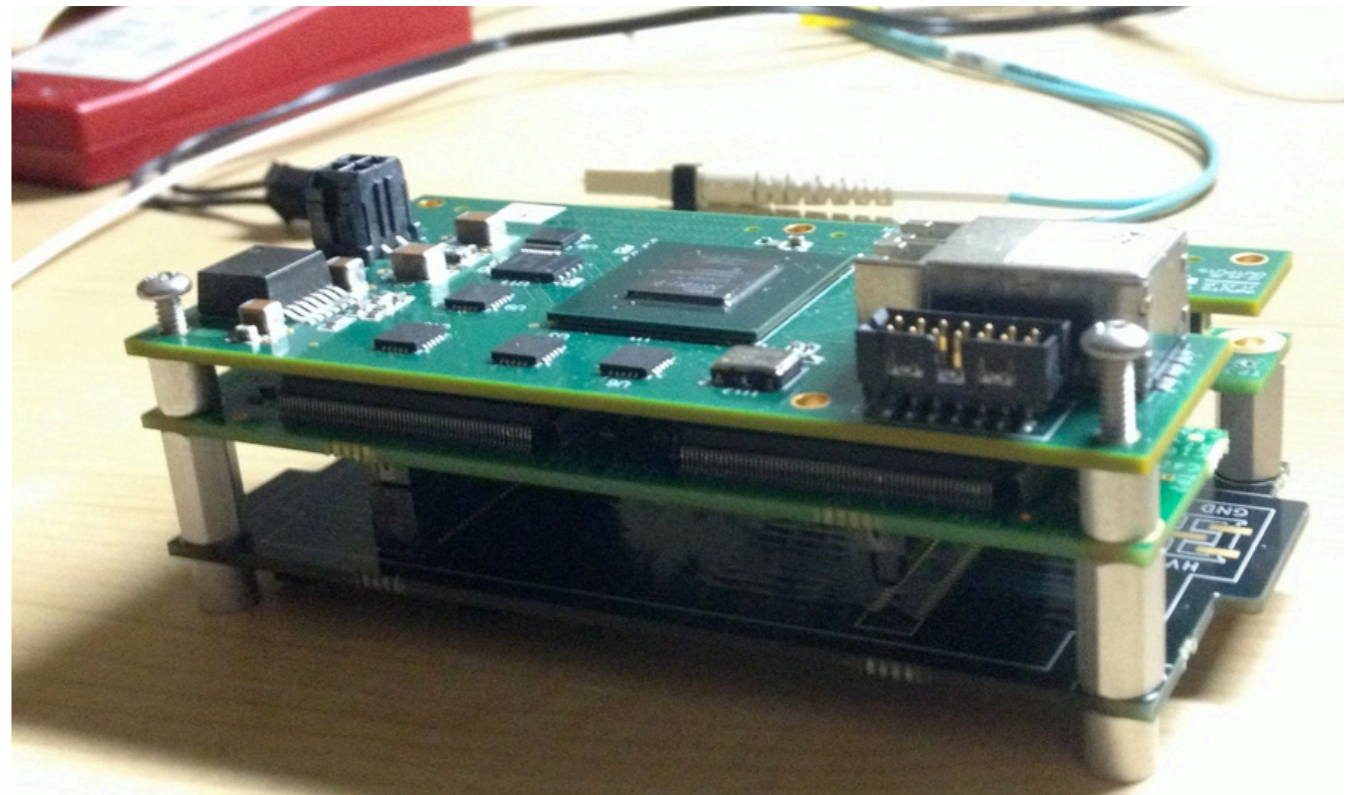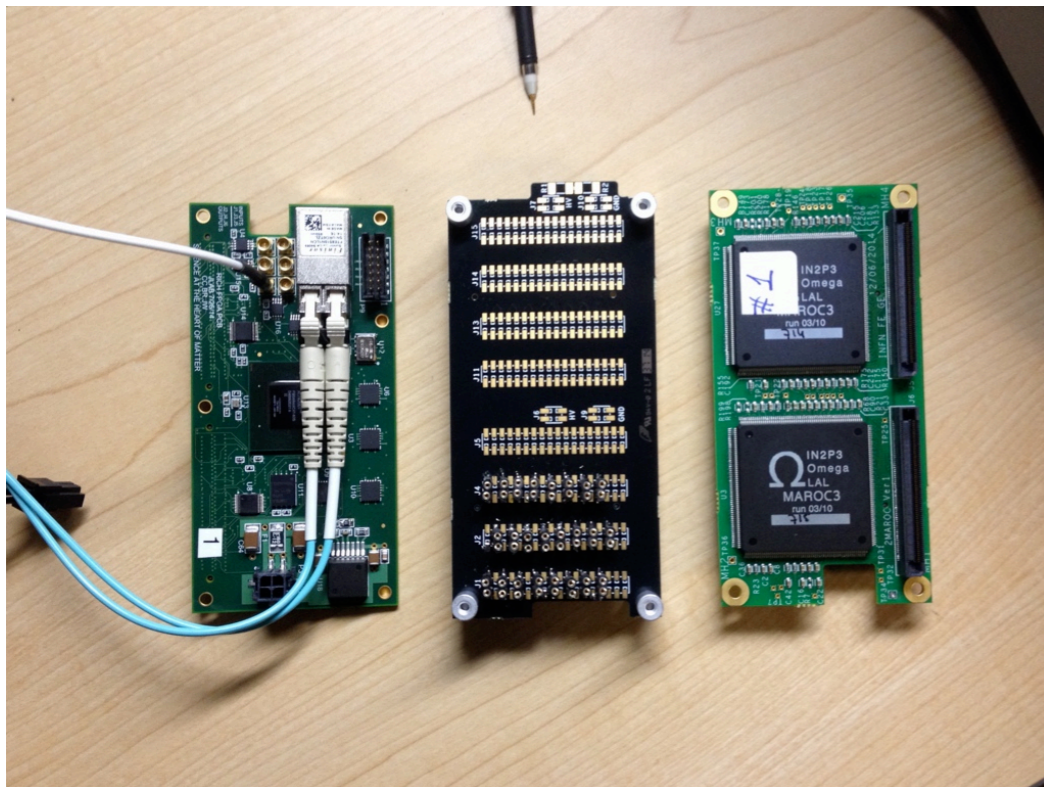
ADAPTER board
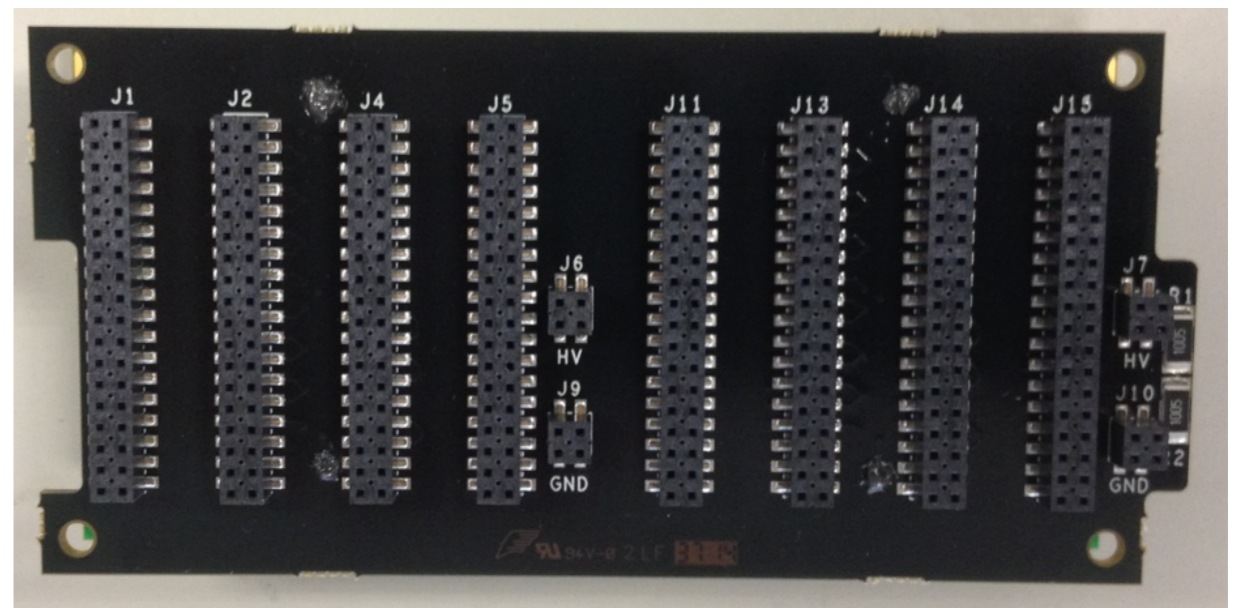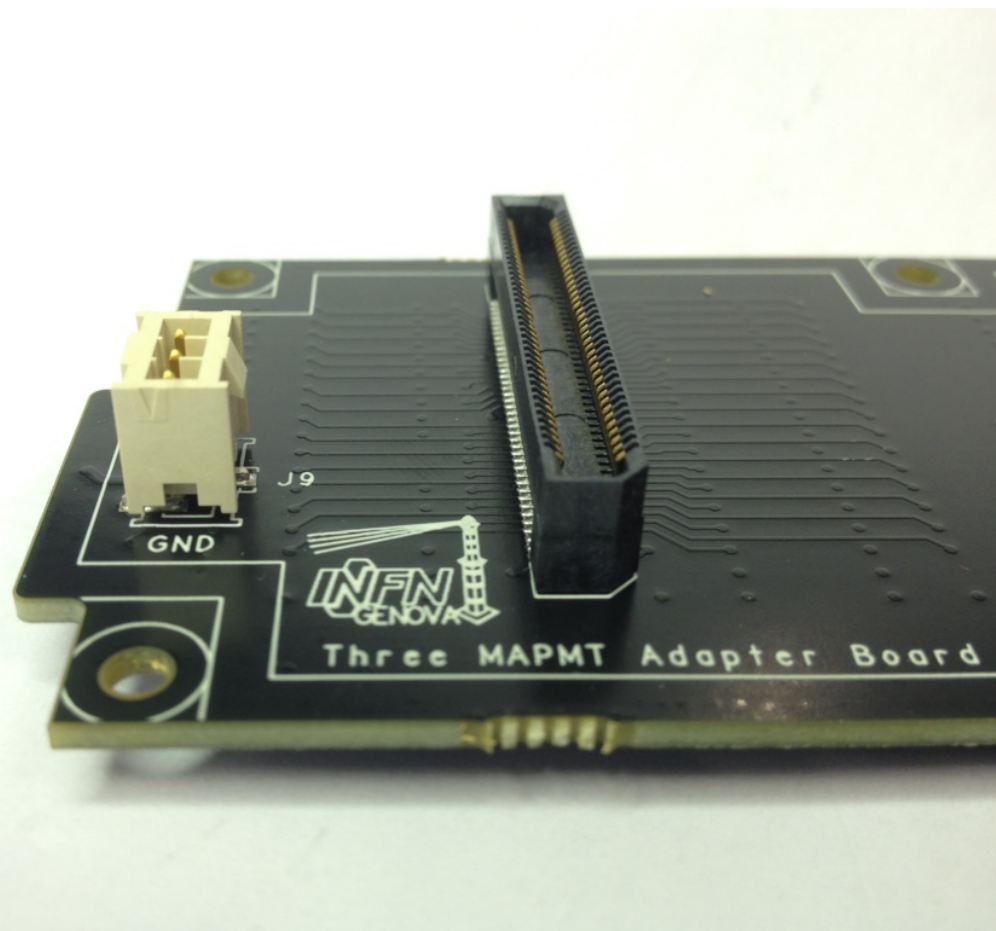
- Passive board

- Light Tight

- Provides HV power to the PMTs and low capacitance electrical connectivity with MAROC

- 16 prototype produced (8 per variant)

- mechanical, electrical and light tighness tests completed

- 2 boards modified to be used as charge injection board during characterization phase

ASIC board

- Houses the MAROC, Voltage regulator, Test Pulse circuit, External ADC,

- Provides interface with MAPMT and FPGA

- 2 versions 192 or 128 channels

- ASIC board available from October 2014

- Internal pulser revised June 2015

- 4 prototypes produced

- Electrical tests passed

- Slow Control completed

- Characterization completed

- TDC readout completed

- ADC readout in progress
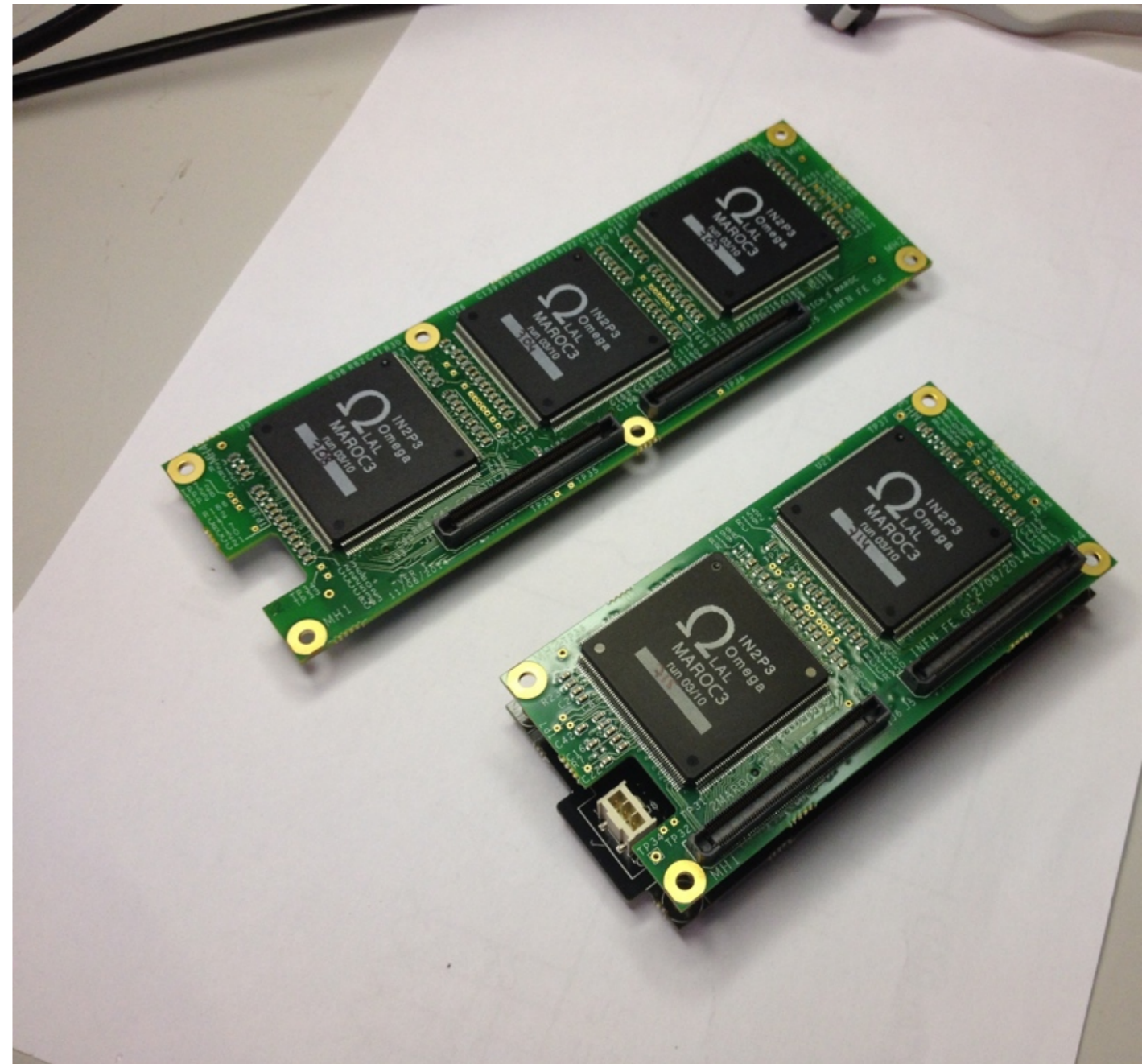
FPGA board

- FPGA board provides the following features:

  - Support 2 or 3 MAPMT/MAROC

  - 192 channels of 1 ns resolution TDC

  - Single fiber optic interface: TDC reference clock, fixed latency trigger, MAROC slow controls, stream triggered data to event builder

  - Low power (3 MAROC + FPGA+ optical transceiver): 4W for 192 channels

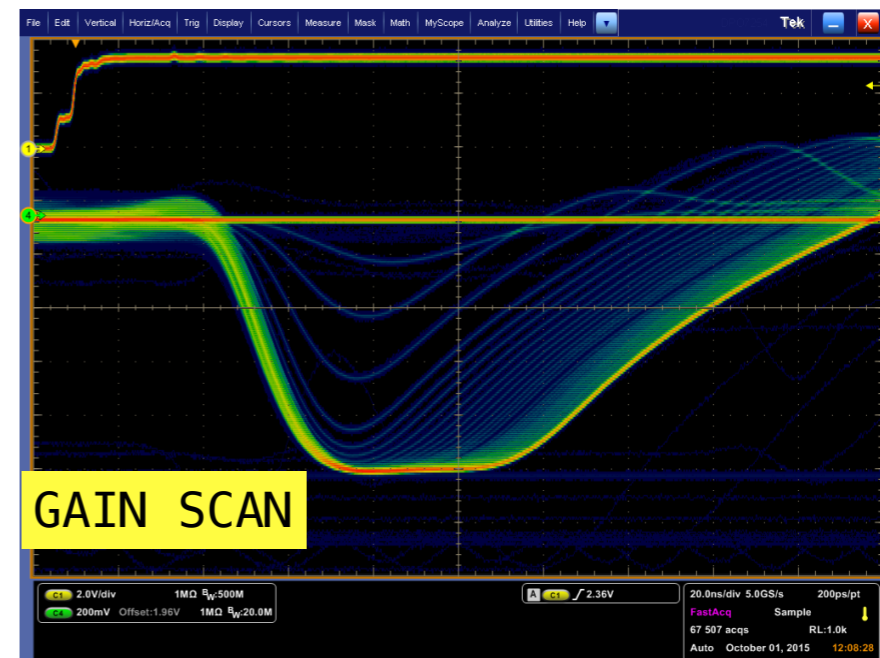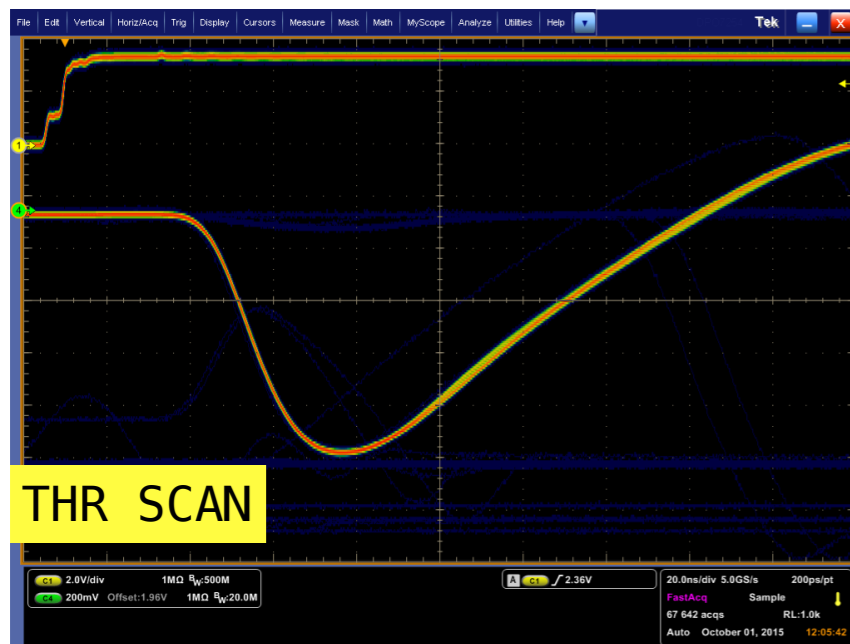 - Interfaces diretly to PC over ethernet (1Gbit) for small setups
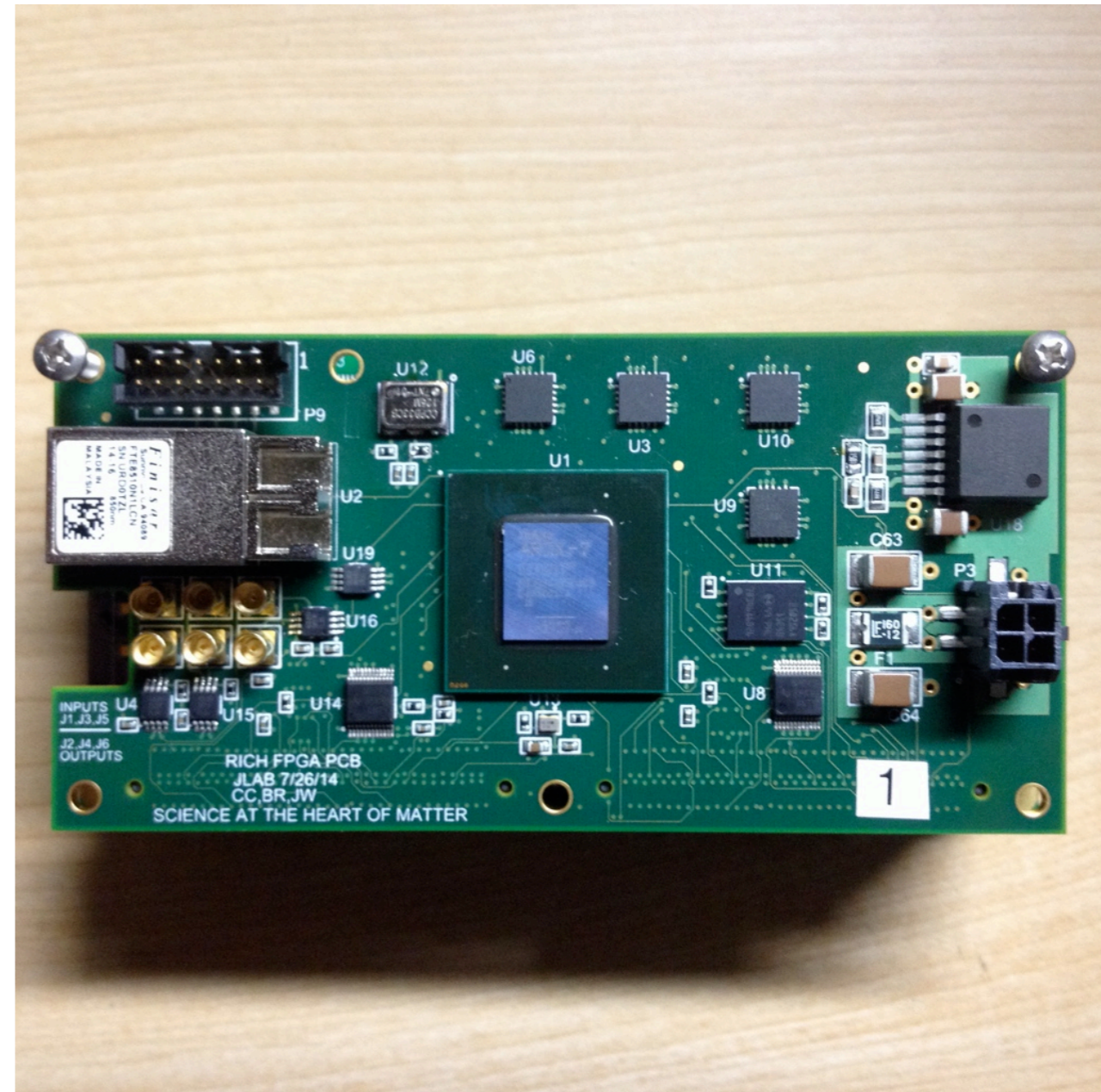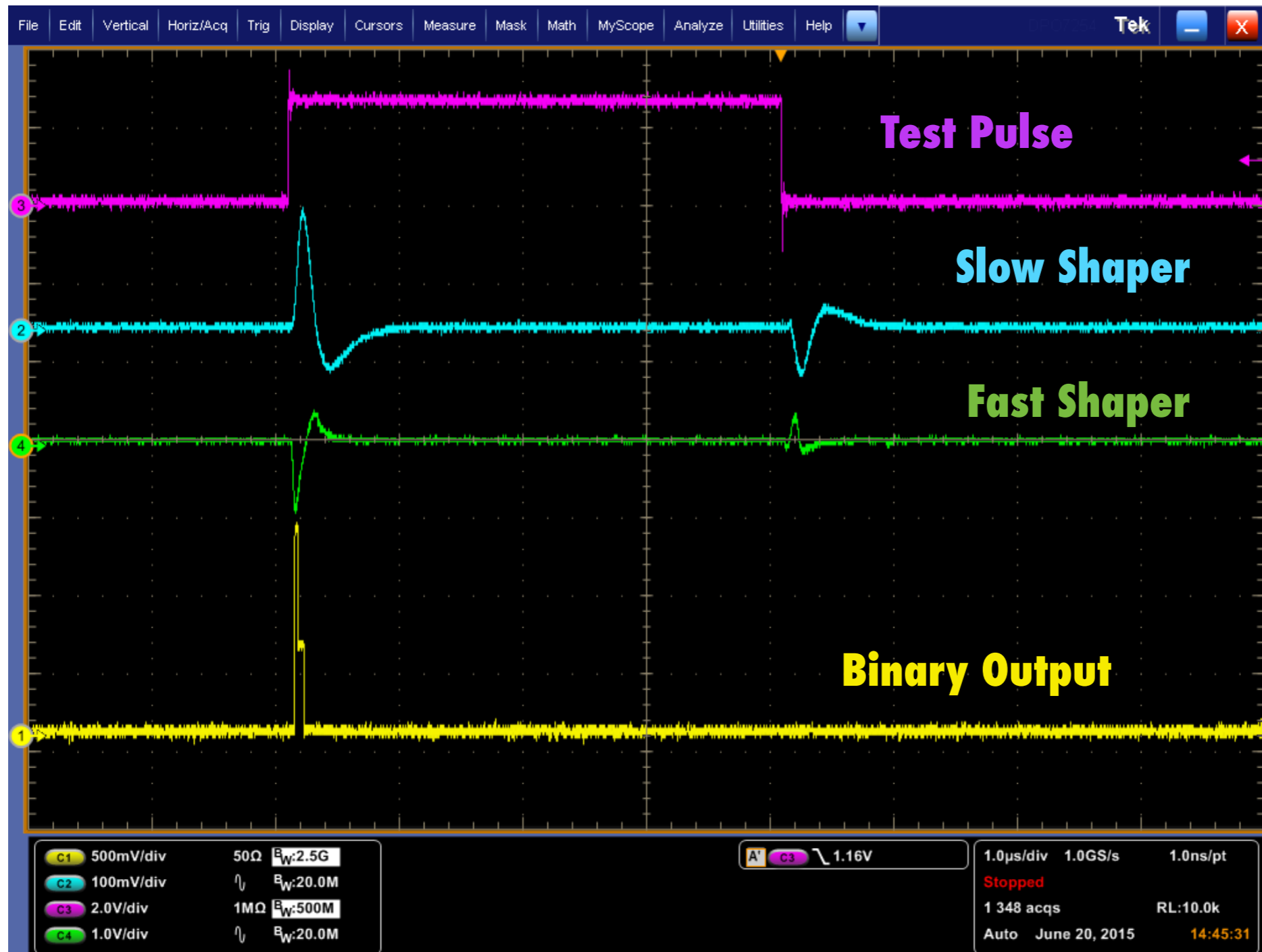
MAROC Fast Shaper response

64 channel fast shaper response

single channel

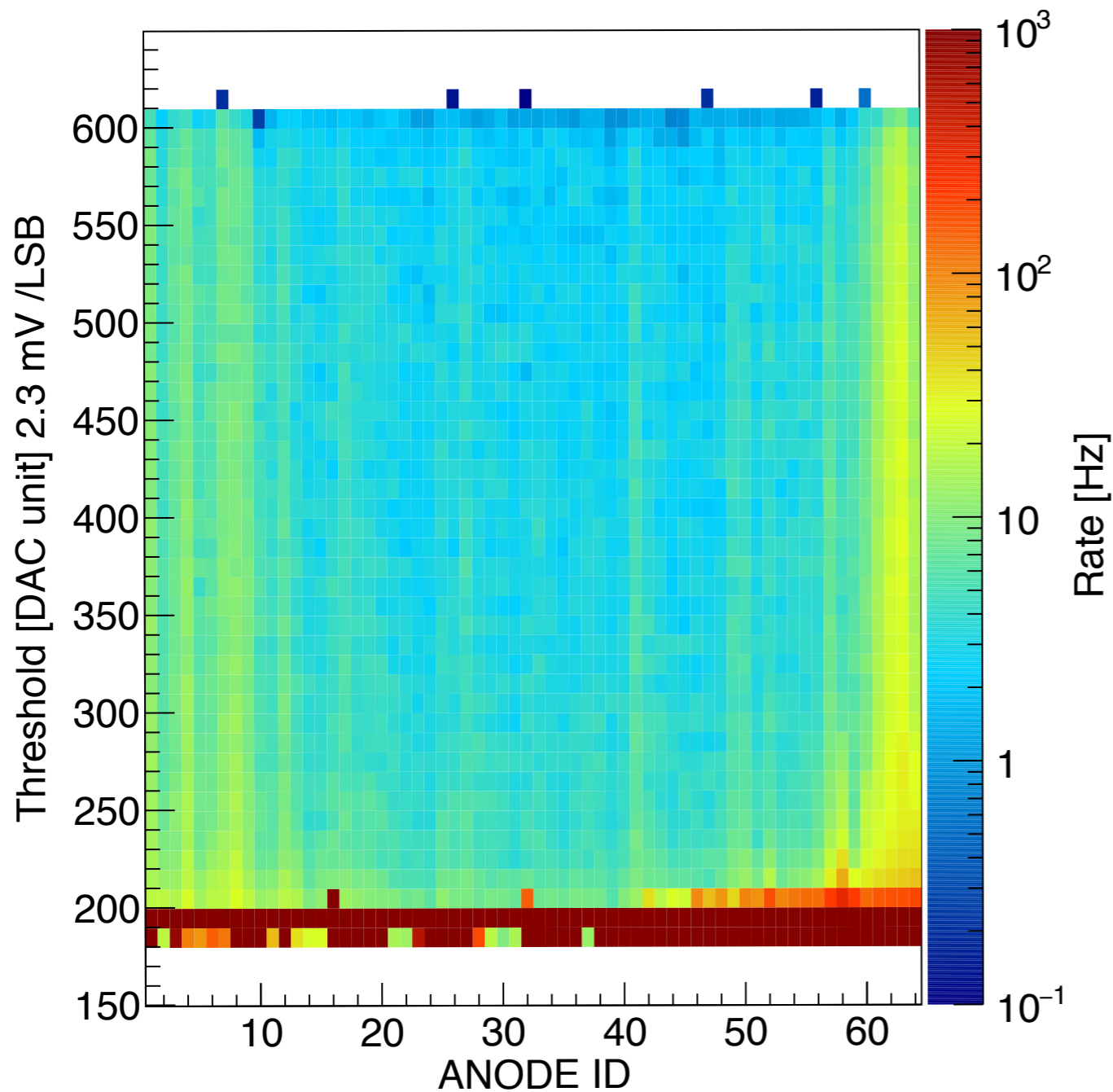

THR SCAN

GAIN SCAN

MAROC analog response

Dark Rate Test

Dark Rate CA7482 HV 1000

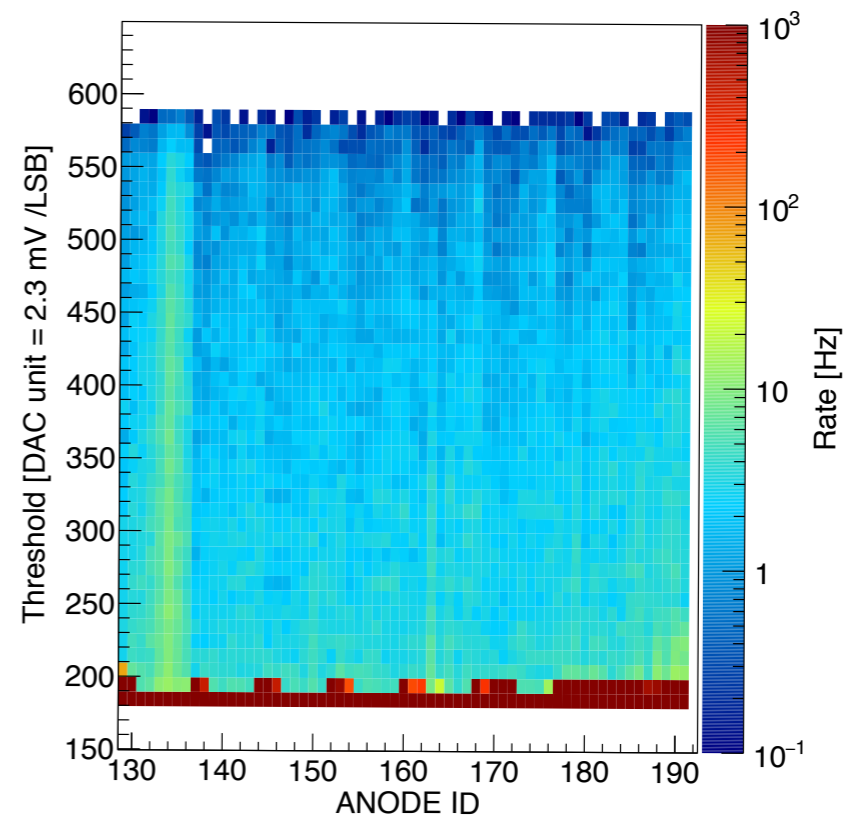Scaler measurements (August 2015, Jlab)

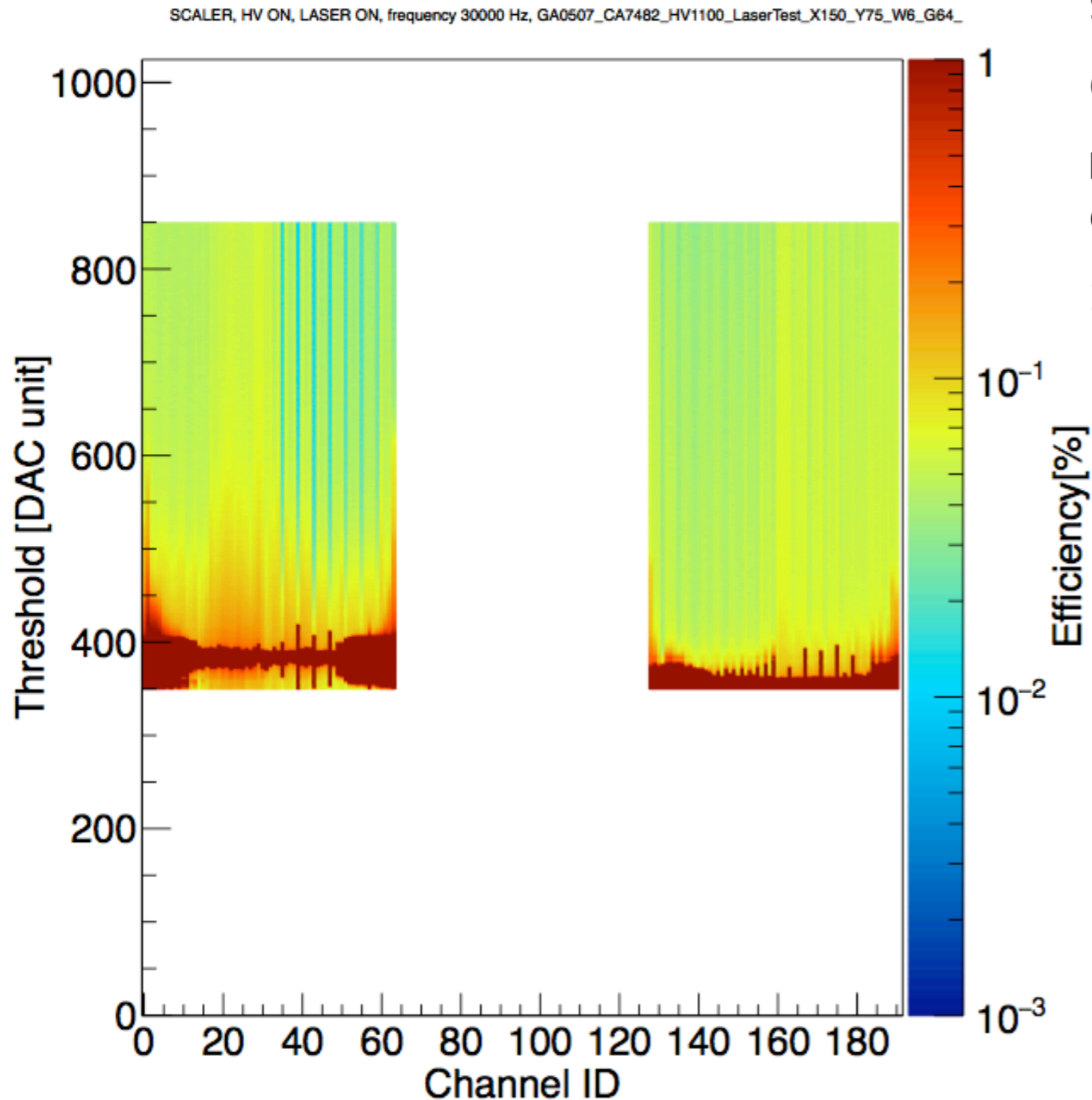Rate compatible with datasheet

Single channel dark rate

Photocathode uniformity

HV and Gain scanned

Dark Rate GA0507 HV 1000
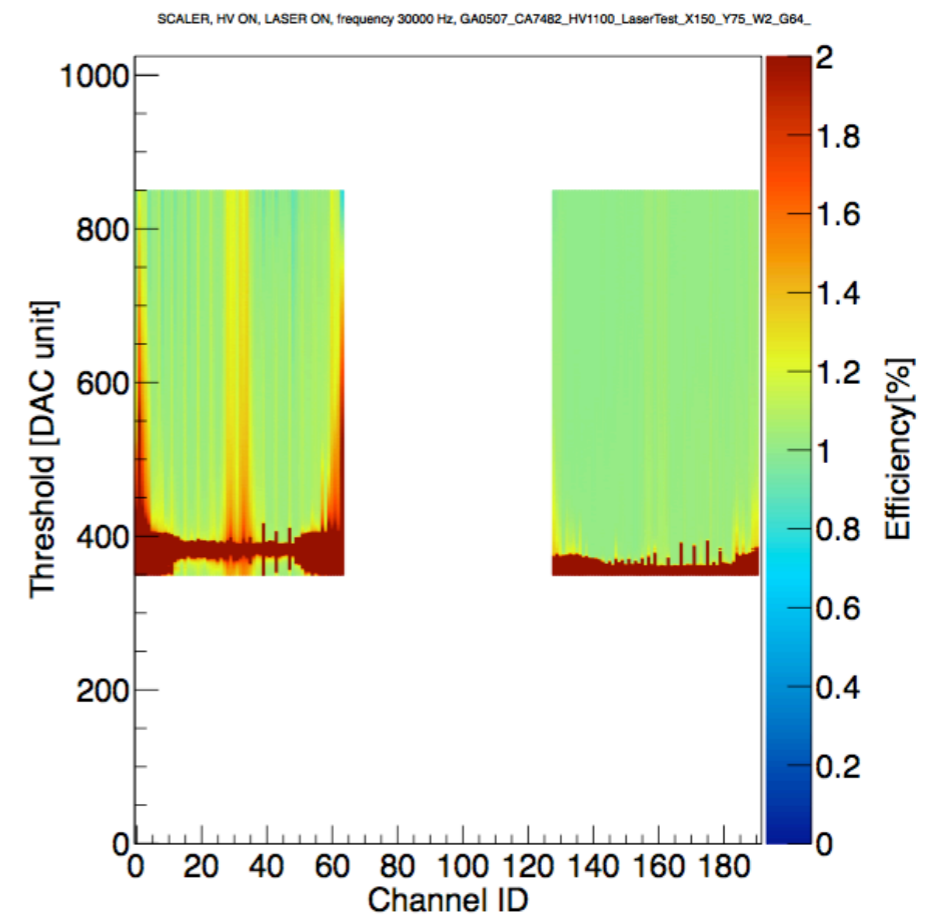
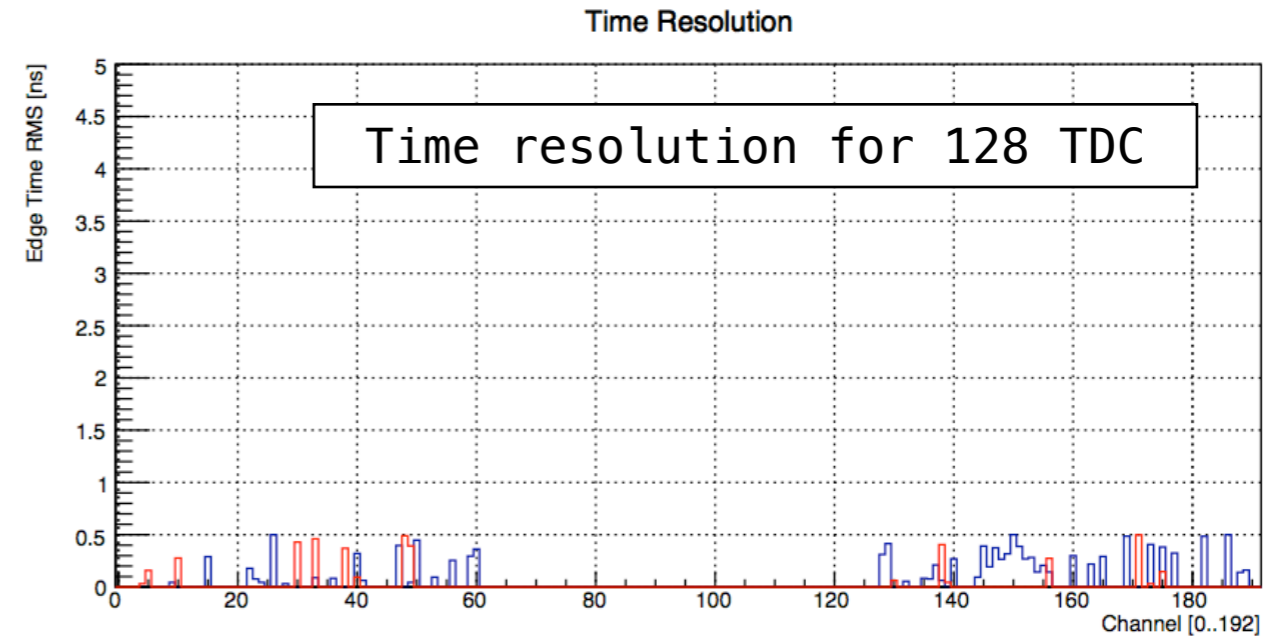# Laser Efficiency Test

Scaler measurements (August 2015, Jlab)
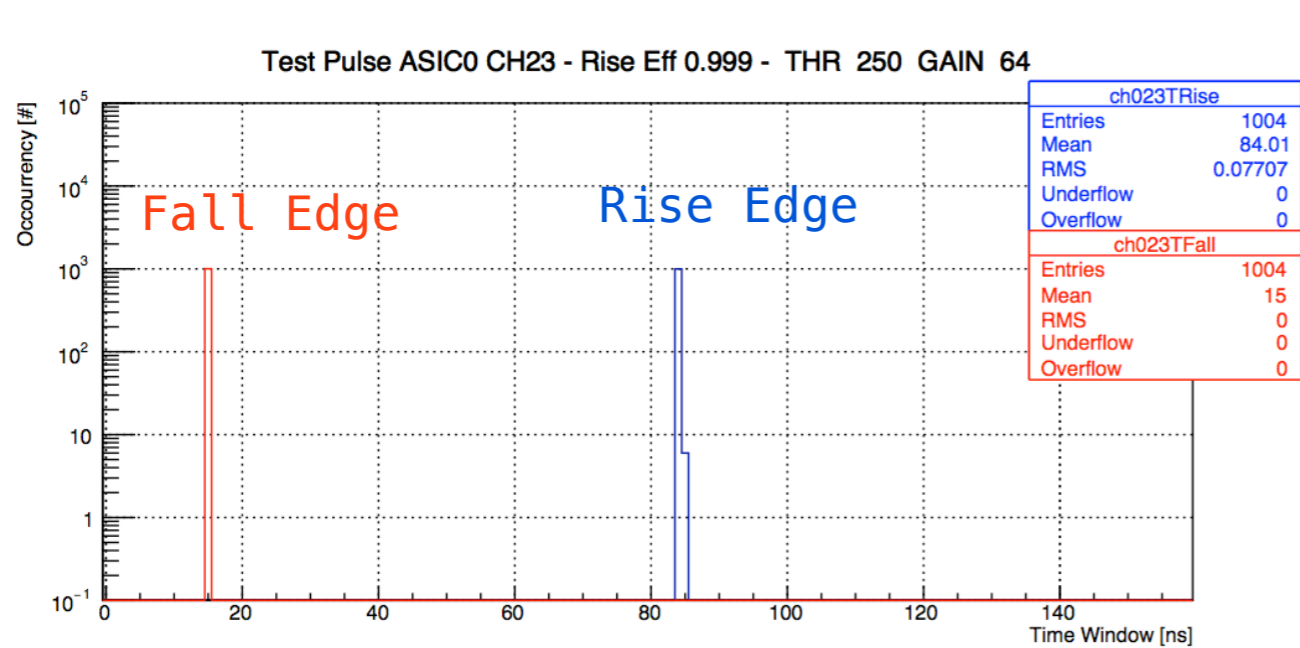
Comparison with fADC measurements

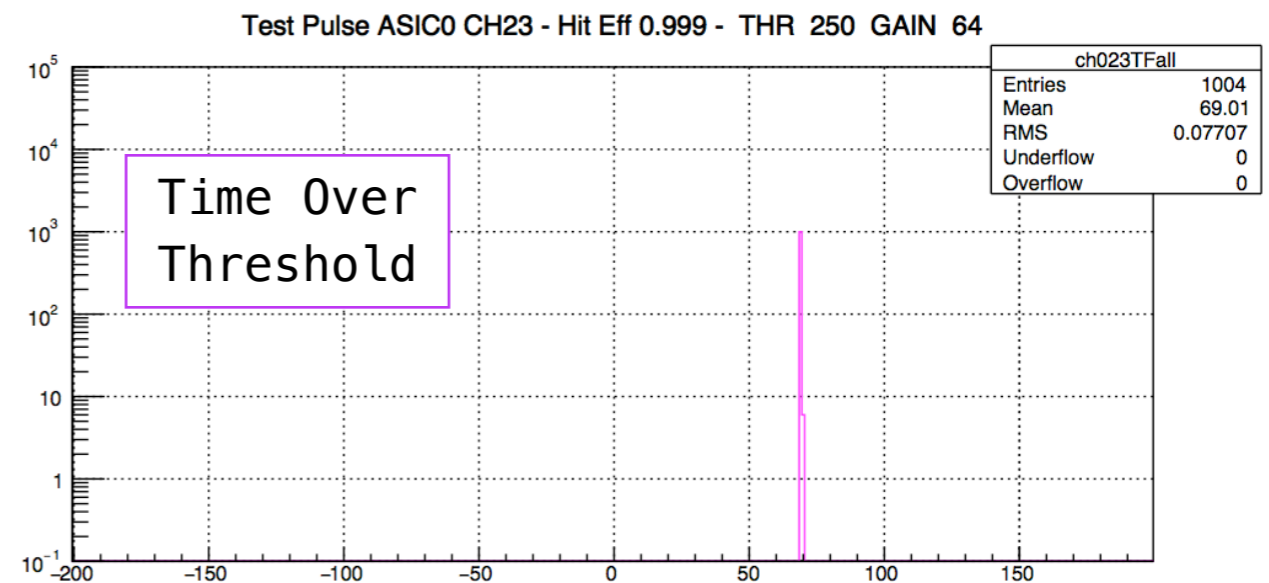HV and Gain, Position scanned for different Light intensity

In the plots 2 different light intensities (single photelectron on the left)

Time Resolution

- Test Pulse TDC response

- Time resolution <500ps

- Good Uniformity

- Time over Threshold study in progress

Radiation Tolerance Test

- Poor data availbale on FPGA, Transceiver

- Equivalent dose 8month

- Monitor SEU, Ethernet link, Voltage regulators, Temperature

- No definitive damage

- No errors on static memory

- Few errors on volatile memory, easy to recover with a power cycle

- Irradiation test will be completed in November

- Analysis in progress
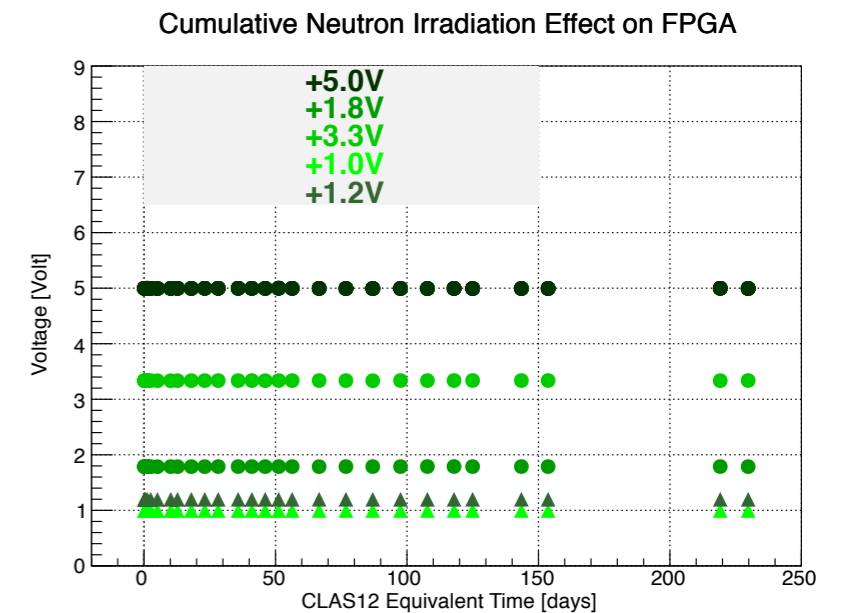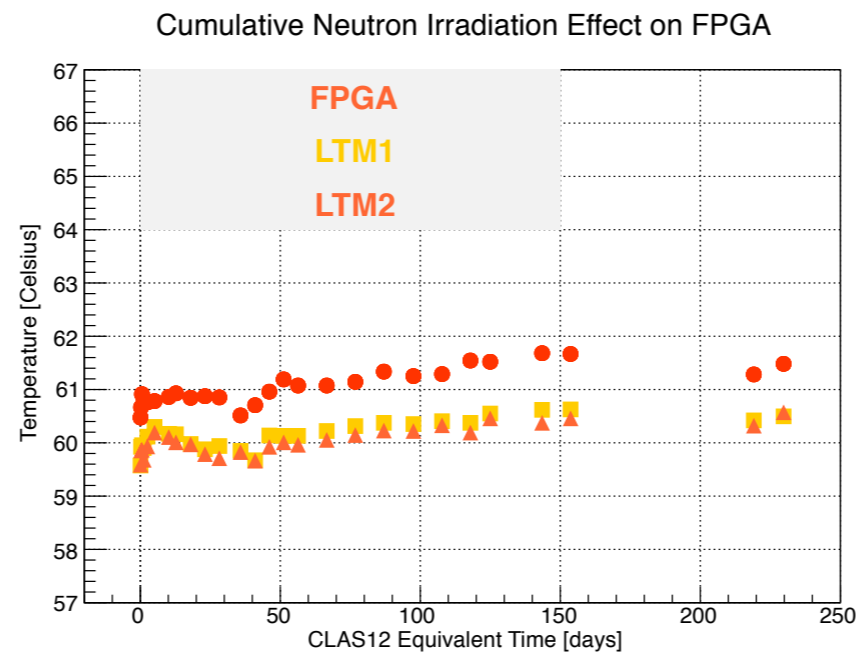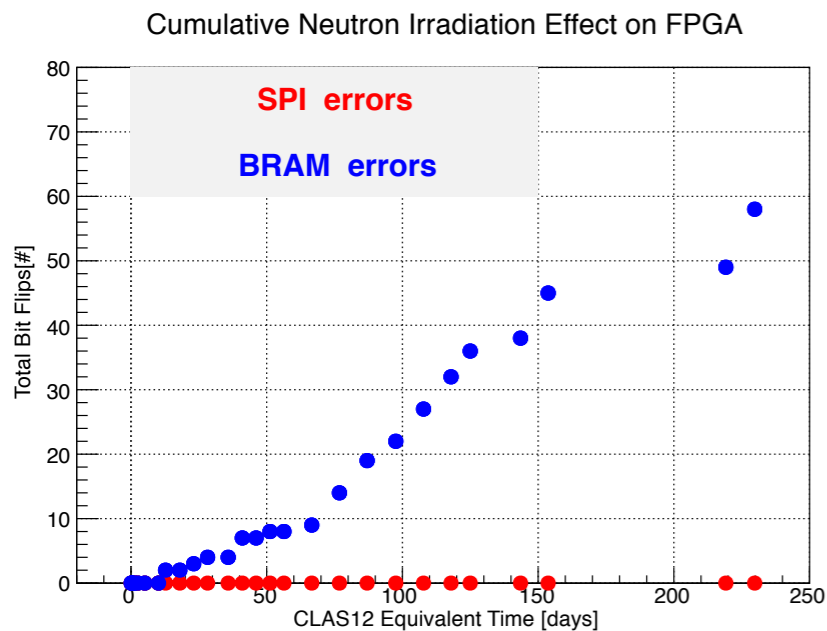
Facility: Frascati Neutron Generator (FNG) Italy

Heat Production
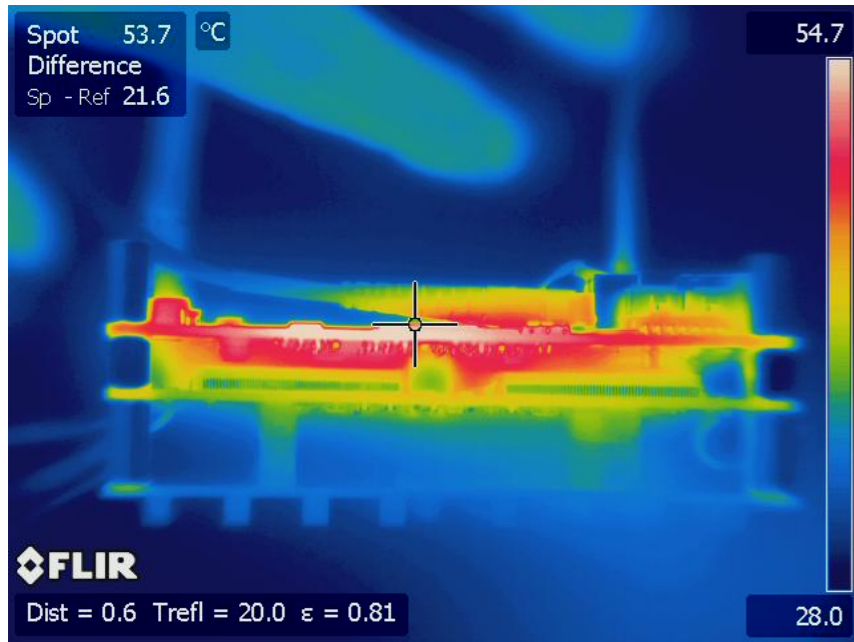
Acceptance Test

Level 0: electrical test and power dissipation (manual)

Level 1: script with diagnostic (automatic)

1. 64 channels input + test channel

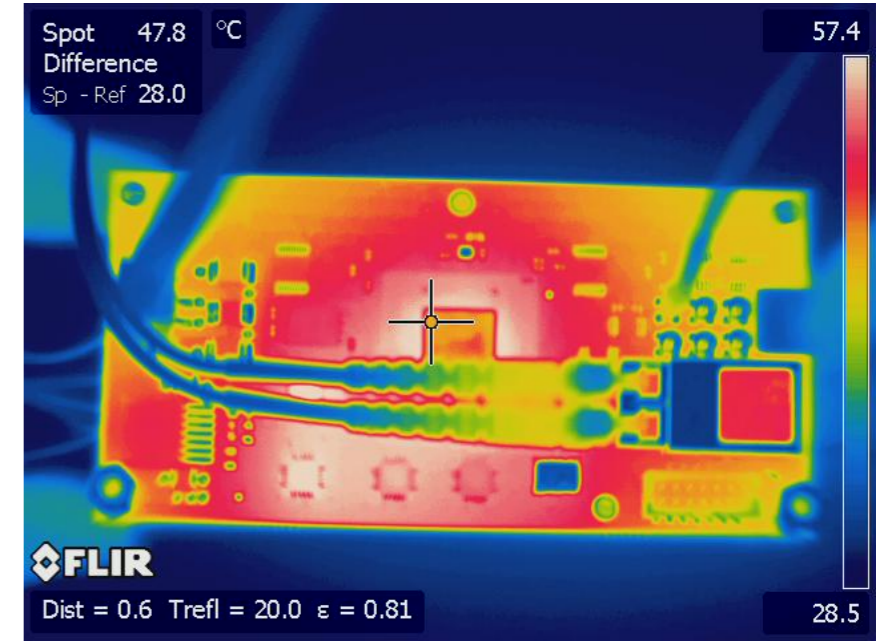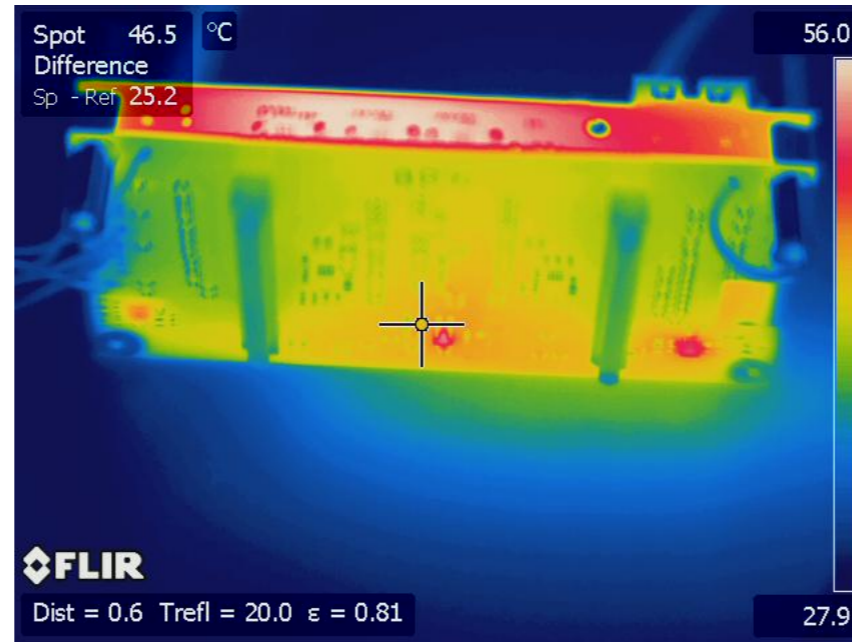2. Slow Control check (gain,shaping,threshold, masked OR)

3. Binary outputs 100% efficiency at 50 fC (1/3 photoelectons)

4. Time resolution (<500 ps expected)

5. Charge response in range 50fC 1000fC

Hardware Requirements: FPGA board, Injection Board, External Pulser

NOTE1: Preamp gain = 0 allow muting unwanted channels

NOTE2: External pulser driven by FPGA board for synchronization

RICH DAQ in CLAS12

MAPMT "Tiles"
Two Tile Types:
2MAPMT per Tile
Or
3MAPMT per Tile
(138 Tiles per sector)
408 Total MAPMT

MAPMT Tile & Cable Support Board
HV, Low Voltage, Fiber Optic

408 - MAPMT
64 Anodes each
26,112 pixels

SSP (VME/VXS) (QTY 5)

MAPMT → ASIC → FPGA → Fiber Transceiver

Up to 300feet (OM3 fiber optics)

SSP → CPU → To event builder

VME64x

Module designed for RICH

Existing CLAS12 DAQ modules
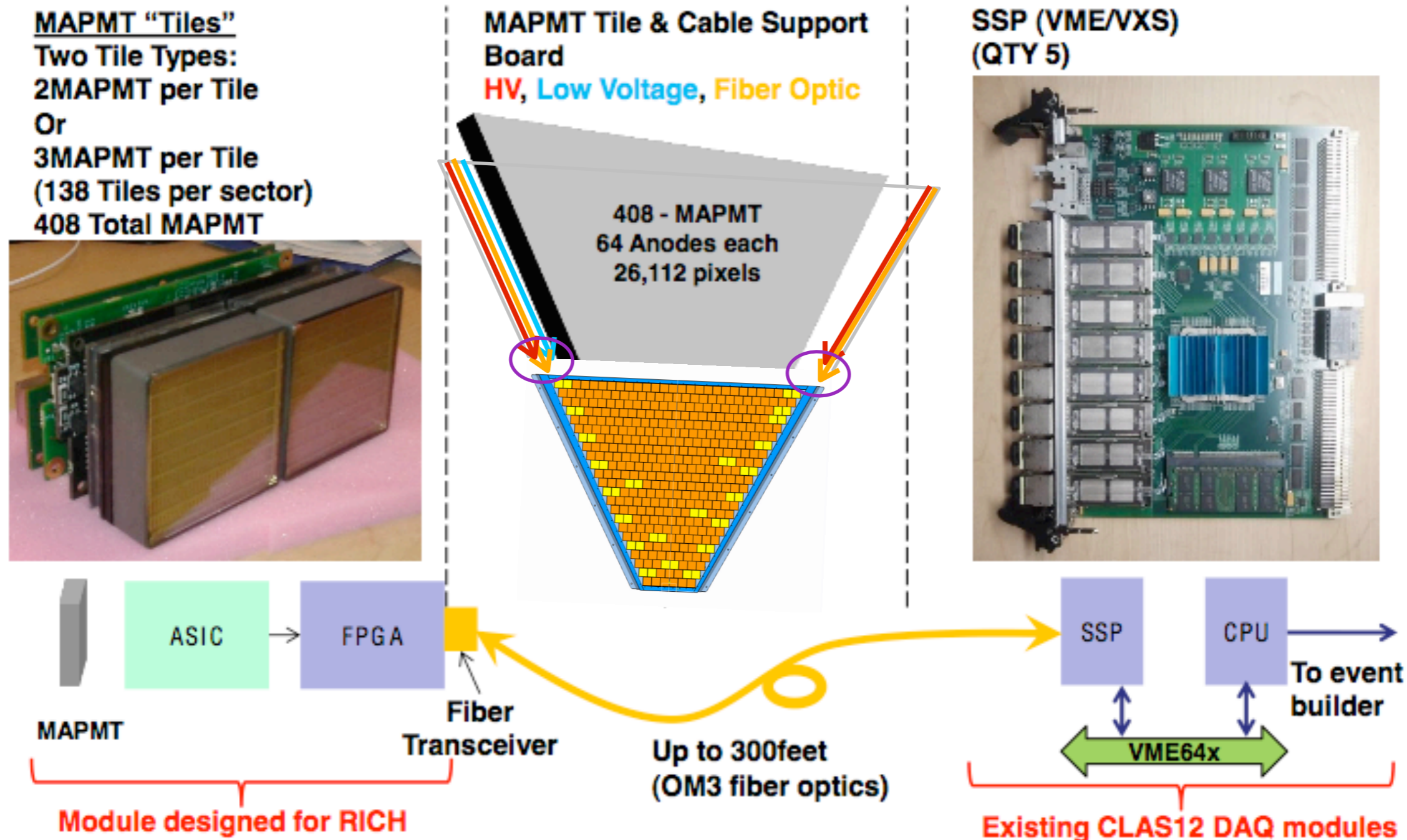
Service scheme

- Different solutions developed to fit in CLAS12 with minimum impact

- Total cabling section 4000 mm2

- Patch panels design complete

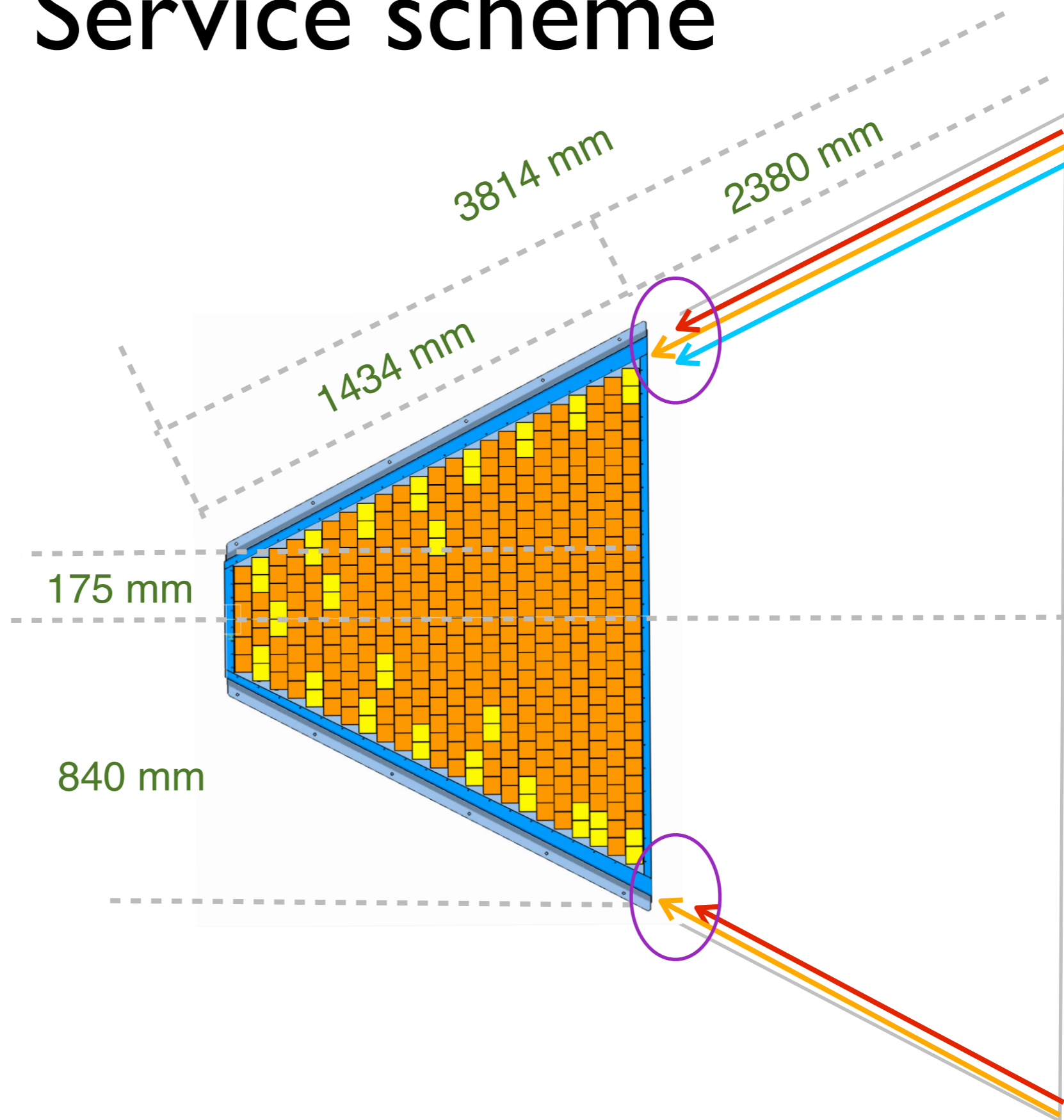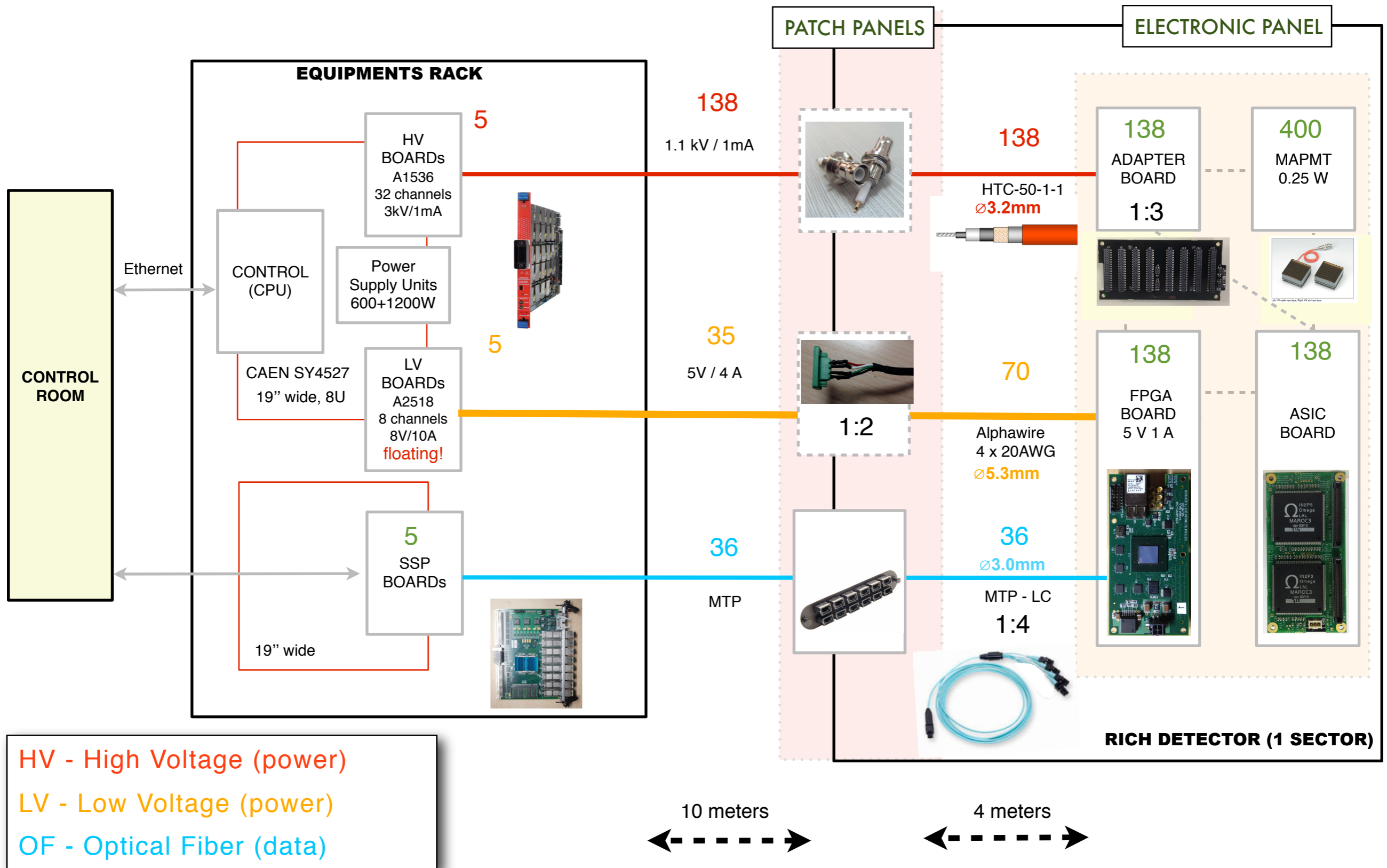- Cable routing on electronic panel in progress

3814 mm

2380 mm

1434 mm

175 mm

840 mm

Service scheme diagram

Status

- Design completed

- Prototype produced and tested

- TDC satisfy the requirements

- ADC part in progress

- Tiles satisfy all the requirements

- Procurement completed

- Production plan completed

- Acceptance test with Charge injector board

- Characterization and Calibration protocols in progress

Summary

Title

- **Design** completed in 2014/07

- **Prototype production** in 2014/09

- **Slow Control** in 2014/11

- **Services** completed 2015/02

- **Test Pulse** completed 2015/05

- **TDC** completed 2015/06

- **Software** completed 2015/08

- **Radiation Tolerance** 2015/09

- **ADC** in progress

- **Acceptance protocol** in progress

- **Characterization protocol** in progress

- **Calibration protocol** in progress

Title

- ASIC board provides the following features:
  - Interface with 2 or 3 MAPMT trough an adapter board
  - Direct connection to FPGA board
  - Test Pulse shaper circuit
  - External ADC
- HW prototype completed in September 2014
  - 4 units produces
  - Software Library completed in July 2015

Test

- Library and script completed August 2015 (C++,ROOT,bash)

- Dark Rate and Laser Efficiency

- Time response

- Time resolution with MAPMT

- Validation and Characterization protocol in progress

- Calibration and monitoring protocol in progress