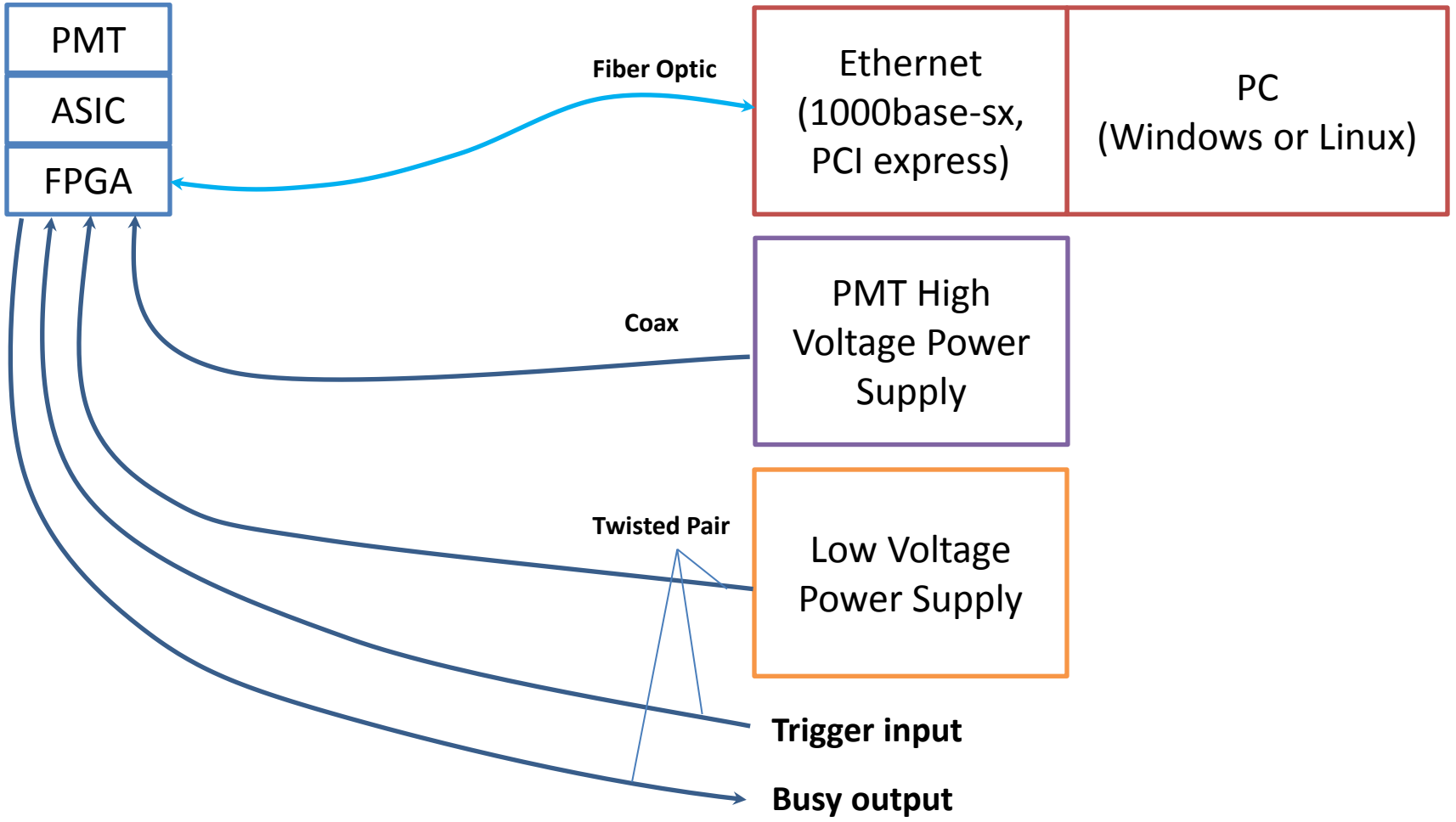
RICH DAQ Prototyping Hardware



RICH DAQ Prototyping Firmware/Software

PMT/ASIC/FPGA Assembly:

- x2 or x3 PMT version
- Digitized MAROC3 analog signal (if ADC is implemented)
- 1ns TDC on MAROC3 digital signals
- 1ns TDC on trigger input (needed since it will be asynchronous in this test setup)
- FPGA is configured via 1000base-sx ethernet port from the PC
- FPGA sends triggered TDC events to PC via 1000base-sx ethernet

PC/Ethernet:

- Standard ethernet interface used to PMT assembly simplifies driver development on both ends
- UDP packets will send configuration packets to the PMT assembly (MAROC3 configuration, TDC windows, enable/disable trigger, etc…)
- UDP will be received from PMT containing triggered events (data would contain: trigger number, timestamp, MAROC3 hit timing measured against trigger input, and optionally digitized pulses if the MAROC3 analog output is digitized.
- Supported trigger rates would be very high (MHz range) due to large available bandwidth on ethernet.
- PC can perform real-time analysis or just write data to file for later offline analysis.