Signals exchanged between various board

Paolo Musico - 23 Jan 2014

Support Board, for each PMT:

- PMT side connectors:
  - n. 4 Samtec TLE-118-01-G-DV for H-8500 signals
  - n. 2 Samtec TLE-102-01-G-DV for H-8500 HV (1 for HV, 1 for HV-RETURN)
- ASIC board side connectors:
  - n. 1 Samtec ERF8-040-07.0-L-DV-K for H-8500 signals (64 + 16 GND)
  - n. 2 Samtec TLE-102-01-G-DV for H-8500 HV
  - Check if all HV connectors are needed or only one couple is enough!
  - Check how to connect GND to HV-RETURN

ERF8-040-07.0-L-DV-K on Support Board mates with ERM8-040-09.0-L-DV-K on ASIC Board with stacking height of 16 mm.

Signals exchanged from ASIC board and FPGA board

From	To	Name	Level	Max number	Notes
asic	Fpga	maroc_hit	HSTL	64×3 = 192	
asic	Fpga	maroc_out	analog	1×3 = 3	4
fpga	Asic	D_R	LVTTL	1	2
fpga	Asic	CK_R	LVTTL	1	
fpga	Asic	RST_R	LVTTL	1	
asic	Fpga	QBUF_R	LVTTL	1×3 = 3	3
fpga	Asic	D_SC	LVTTL	1	1
fpga	Asic	CK_SC	LVTTL	1	
fpga	Asic	RST_SC	LVTTL	1	
asic	Fpga	QBUF_SC	LVTTL	1	1, 3
fpga	Asic	HOLD1	LVTTL	1	5
fpga	Asic	HOLD2	LVTTL	1	5
fpga	Asic	START_ADC	LVTTL	1	
fpga	Asic	RESET_ADC	LVTTL	1	
fpga	Asic	CLOCK_ADC	LVDS	1 (2 lines)	
asic	Fpga	OUT_ADC	LVTTL	1×3 = 3	
asic	Fpga	TRANSMITON_ADC	LVTTL	1×3 = 3	
asic	Fpga	OR1	LVTTL	1×3 = 3	
asic	Fpga	OR2	LVTTL	1×3 = 3	
fpga	Asic	EN_OTAQ	LVTTL	1	
fpga	asic	CTEST	LVTTL	1	6
fpga	Asic	GND	Power	> 20	
fpga	Asic	+4.0 V	Power	> 10	

Grand total of 225 or 227 pins, without power rails. See Note 4.

Notes:

1. D_SC - QBUF_SC are daisy chained between the 2 or 3 MAROC on the ASIC board
2. D_R is paralleled to the 2 or 3 MAROC
3. QBUF_x can be used to check that the corresponding chain is closed
4. In case to put the ADC (n. 2 or 3) on the ASIC board the 3 pin maroc_out must be replaced with enable, clock, dout of the 2 or 3 SPI ADC. In total change from 3 to 5 pin. In this case the grand total goes to 227 signals
5. HOLDx signals must be delay tuned before connecting to the MAROC. This can be done in the FPGA Board with a programmable delay line or in the fpga itself
6. CTEST must be handled on ASIC Board to provide a known charge to the MAROC inputs

Connectors proposal between ASIC and FPGA boards

Needs of a least 250-260 pins, high density. It could be possible to adopt 2 connectors with 0.5 mm pitch, 130 pin each.

Panasonic AXK5SA3677YG (receptacle), AXK6SA3677YG (socket) pairs, have 130 pins, mating height of 6.5 mm and footprint of 35 mm × 5.4 mm maximum.

As alternative the Samtec ERM5/ERF5-070-02.0-L-DV-K pairs, have 140 pins, mating height of 7.0 mm and footprint of 42 mm × 5 mm maximum, slightly larger than preceding.

In case of use the proposed solution of 2 high density connectors could it be possible to study a FPGA board that fits both the 2 and 3 PMT modules. One size fits all!
Detailed studies must be done with real design implementation.