RICH Latests

RICH installation planned dates as agreeded with Bob Miller:

- August: LTCC sector #4 will be removed from the forward carriage

- September 11 (+1 week of contingency) :
  air compressor, tank, control panel, crates and cables in Hall B

- September 16 (+1 week of contingency) : DSG starts cabling

- October 15 (+1 week of contingency) : RICH in Hall B

Latests

Mechanics: OSP for RICH component installation approved
Support structure installed: good fit to RICH
Several elements being 3D printed at JLab
Design ongoing of the installation brackets (last major item)

Planar Mirrors: All lateral mirrors done, shipment to JLab next week
Front mirrors under production. Shipment to JLab: 18th of September.

Spherical Mirrors: Dispatch from ECI to CMA starts today
Reflectivity of mirror#3 has been measured by DSG at Youri's stand
5 spots: 85% - 90% reflectivity for wavelengths 430nm to 650nm

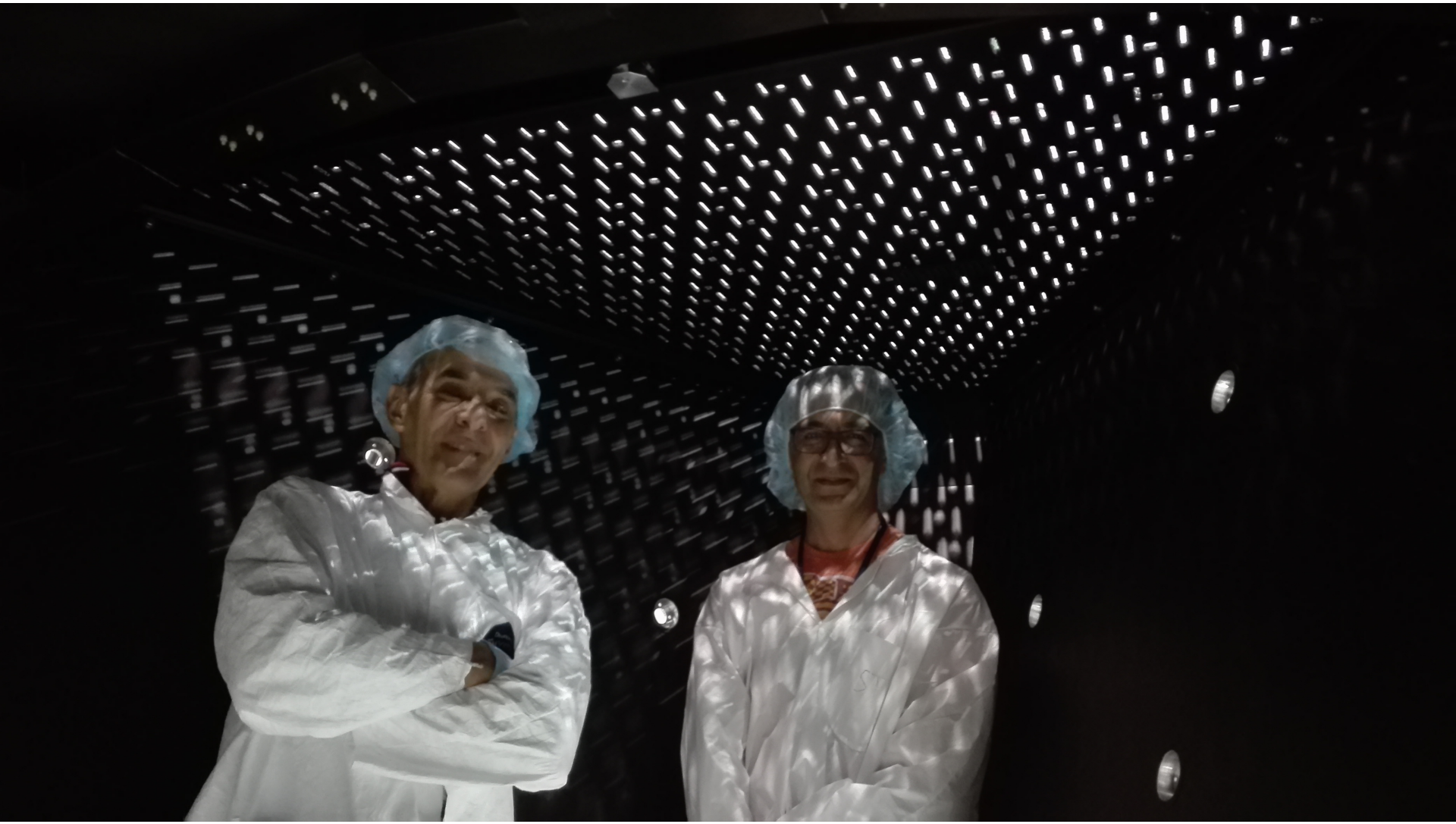
Aerogel: All 2 cm squared tiles ready for dispatch
8 tiles remaining to be shaped

Electronics: 40 F-E units characterized
All MAROC boards (except one) revised by R. Malaguti
Extended TDC tests under way
Cosmic stand installation initiated
SSP firmware pretty advanced (TDC event builder available)

Software: Monitor suite basically ready to play with SSP
Calibration challenge planned in August

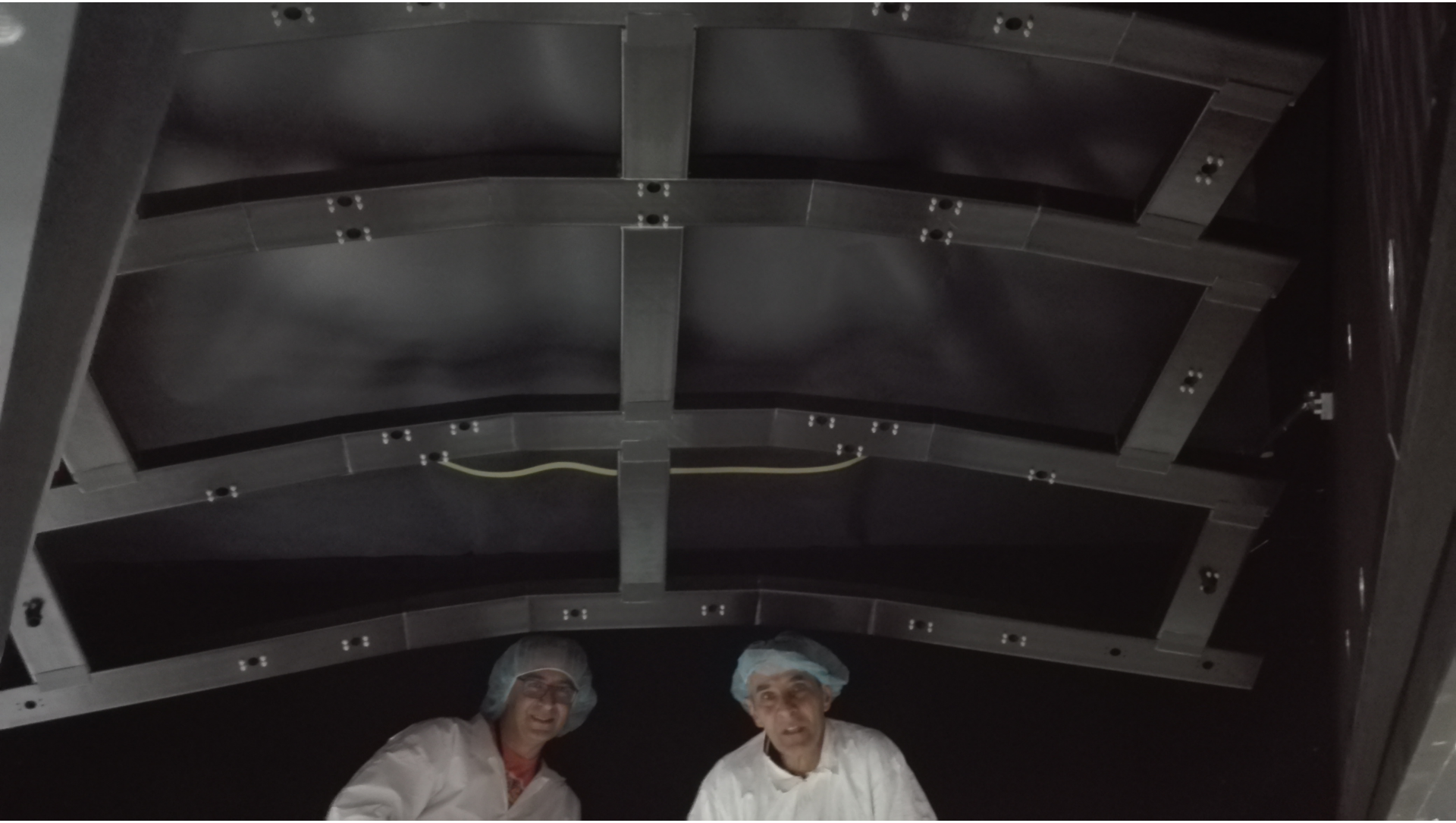
Mechanics

Electronic Panel

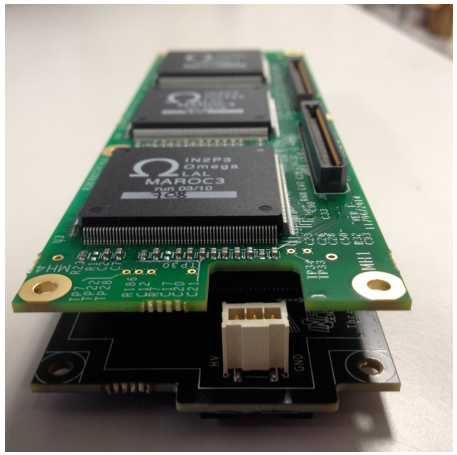


Mechanics

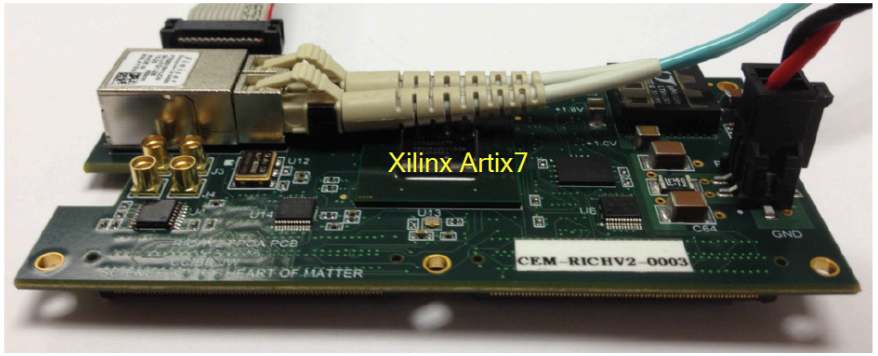
Spherical Mirror Support



RICH Front-End Electronics



In collaboration with FE group



Analog: Charge (1 fC)
Digital: Time (1 ns)

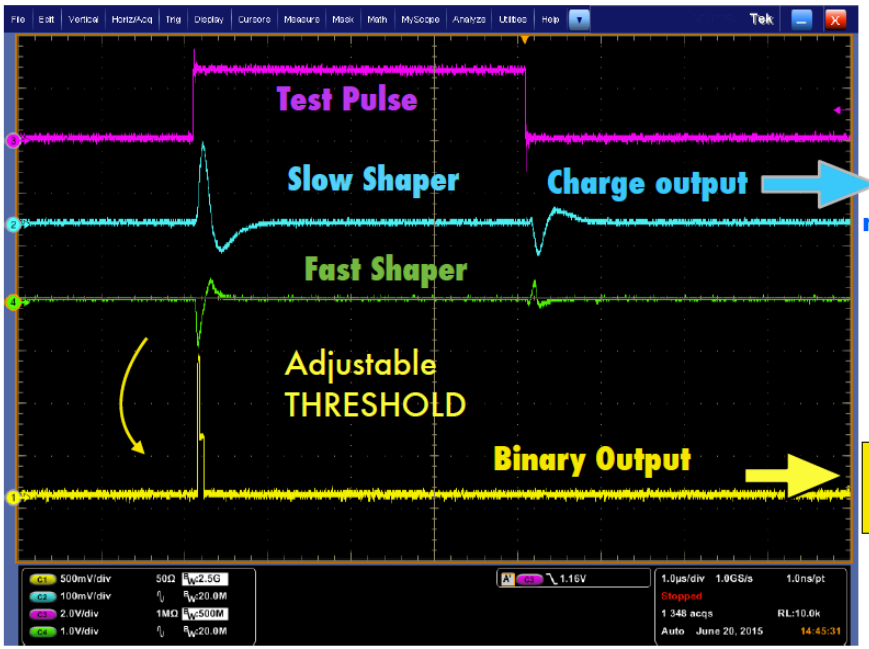
Trigger latency (8 μs)

Optical ethernet (2.5 Gbps)

Trigger: external
internal
self

On-board pulser

example of MAROC signal processing



ADC
(MAROC)
calibration only
more on backup slide

SCALER/TDC
(FPGA)

TDC used for physics runs!

Single channel response, 1 microsecond/div

Calibration

✗ Multiplexed ADC charge measurement LINEAR but only meant as a calibration tool

Can not be used during CLAS12 data-taking (not enough trigger latency, fixed time delay vs TRG)

Parameters as gain, relative and absolute efficiency from LaserTED are useful to validate TDC

Gain = SPE model value fitted from charge spectrum

Relative Eff = Charge spectrum integral above threshold / SPE model integral

Absolute Eff = # events with charge above threshold / # triggers
(assumes uniform laser light illumination)

Necessary to deal with cross-talk (optics and electronics) to avoid over-estimate

✗ Parallel TDC digital readout: NOT-LINEAR but charge estimation

Gain = estimate form time-over-THR spectrum → Required to monitor stability in time

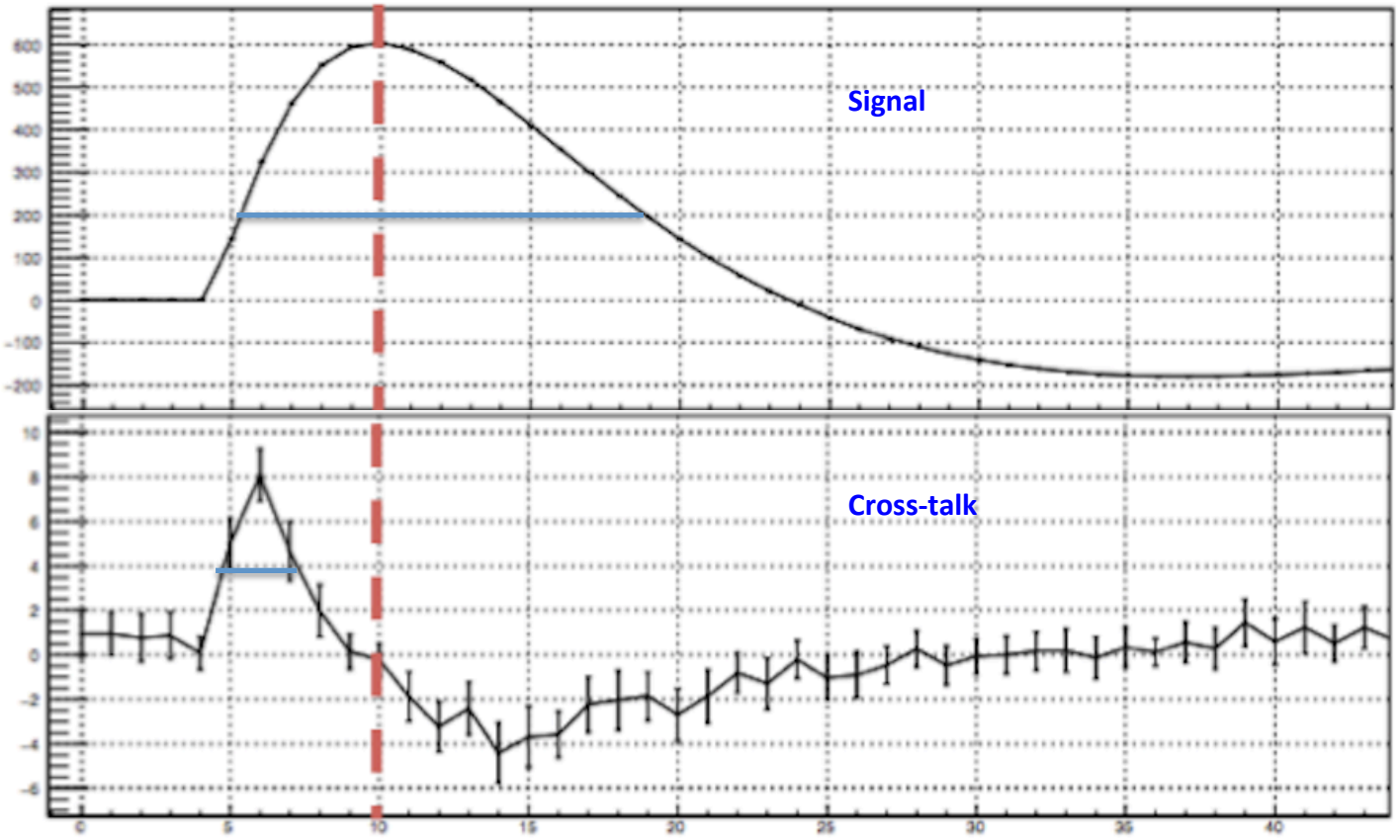
Relative Eff = only possible in comparison to ADC, or to a lower THR

Absolute Eff = # events with charge above threshold / # triggers
(assumes uniform laser light illumination) → Required for Likelihood

Time = 1ns timestamp provided by FPGA → Required for Likelihood

Calibration

ADC **TDC**



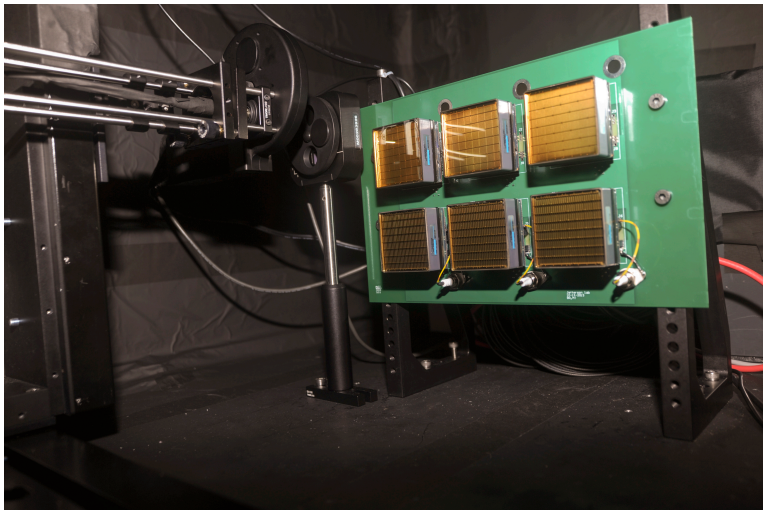
FE Electronics: Charge

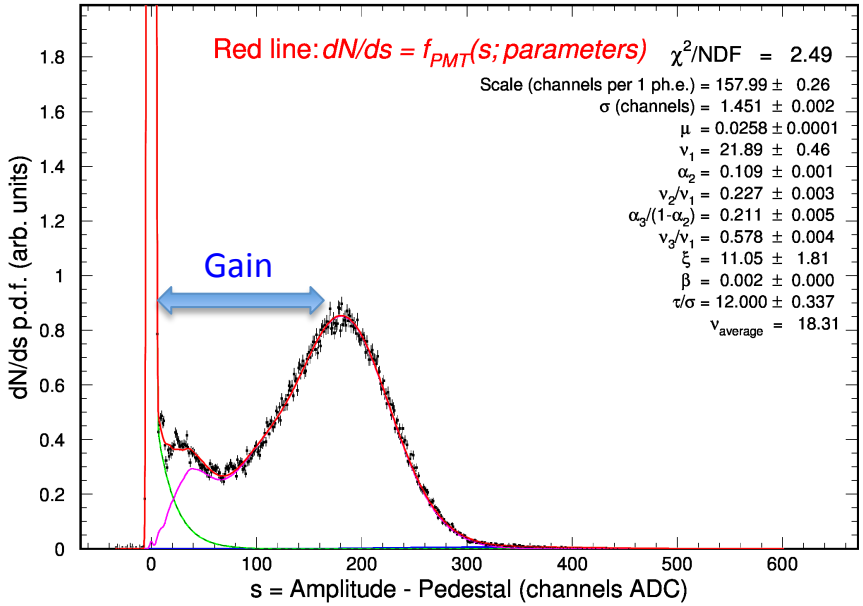
Multiplexed readout up to 50 kHz

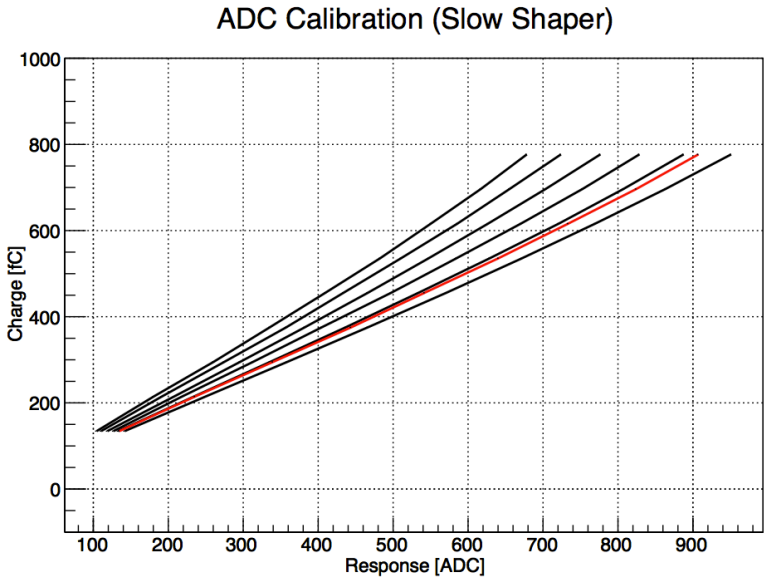
High resolution SPE spectrum

Viable for efficiency and gain monitors

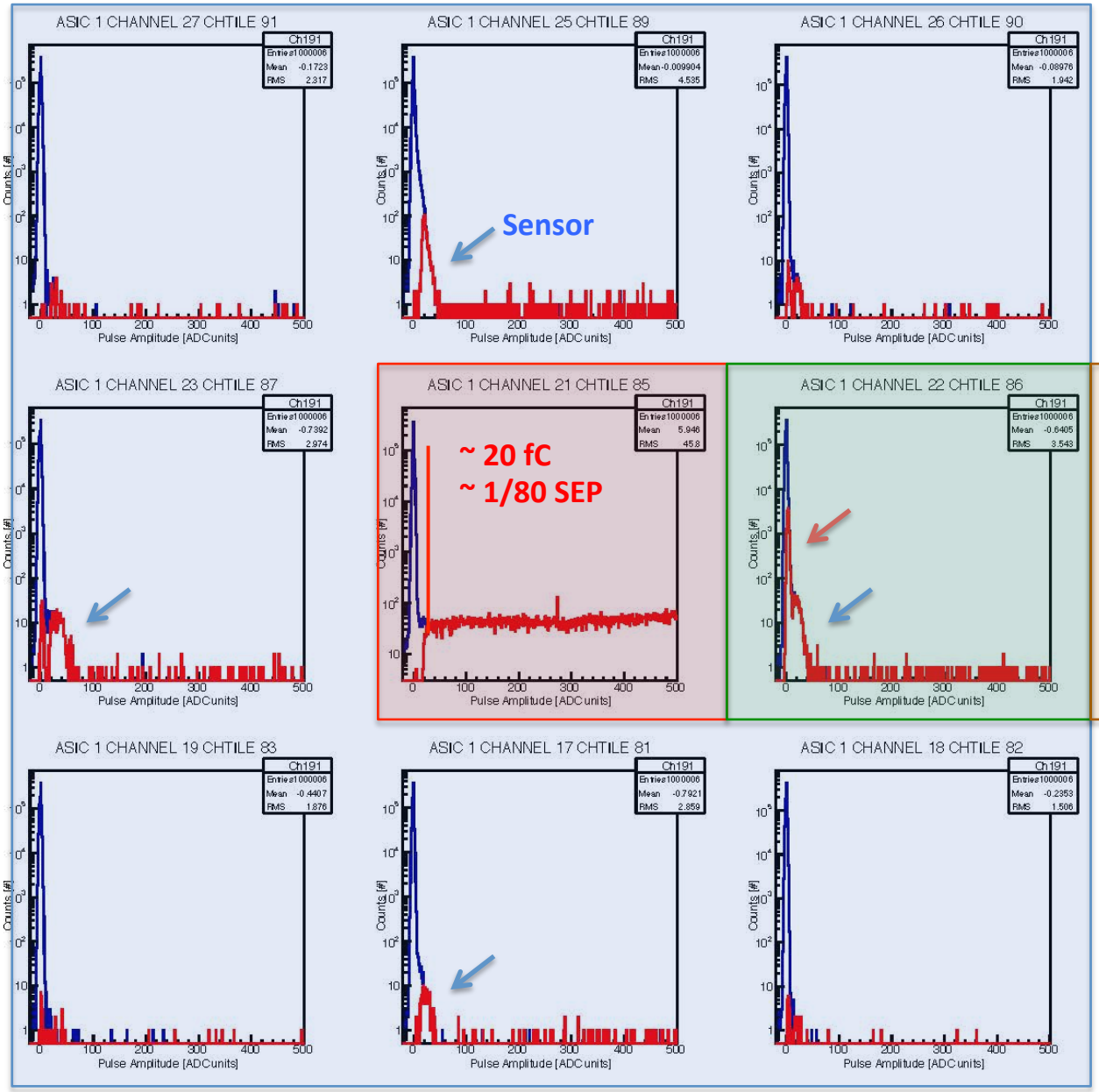
In conjunction with timing, allows the study of PMT discharge and cross-talk





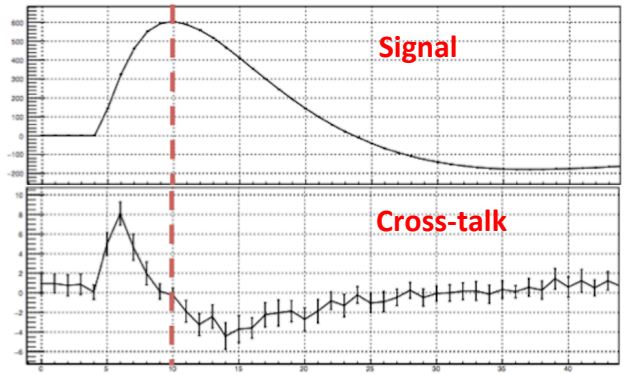


RICH Electronic: Cross-talk

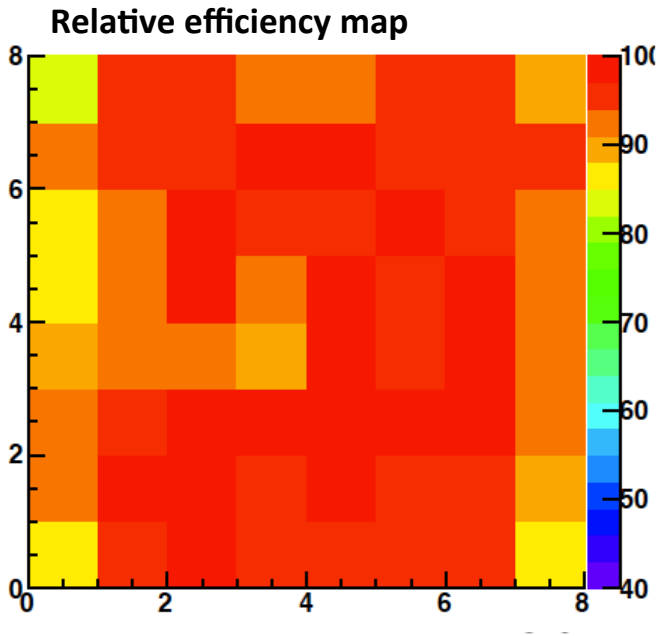


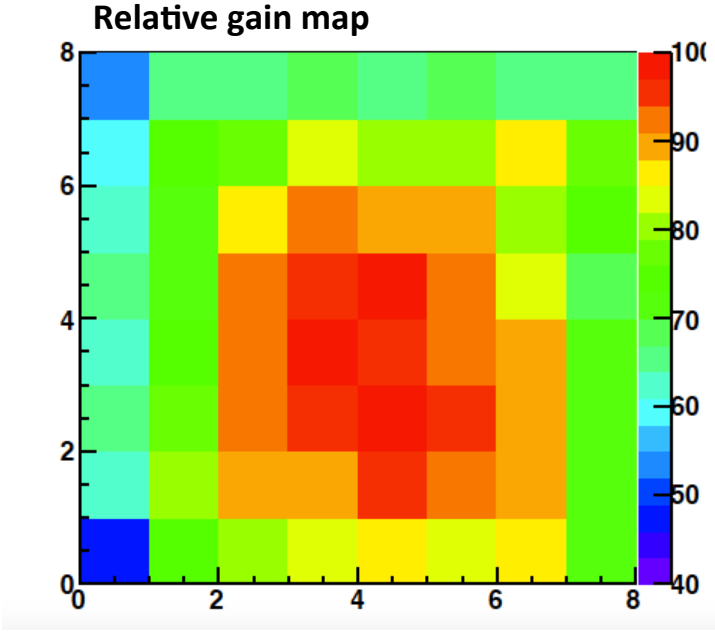
GA0501

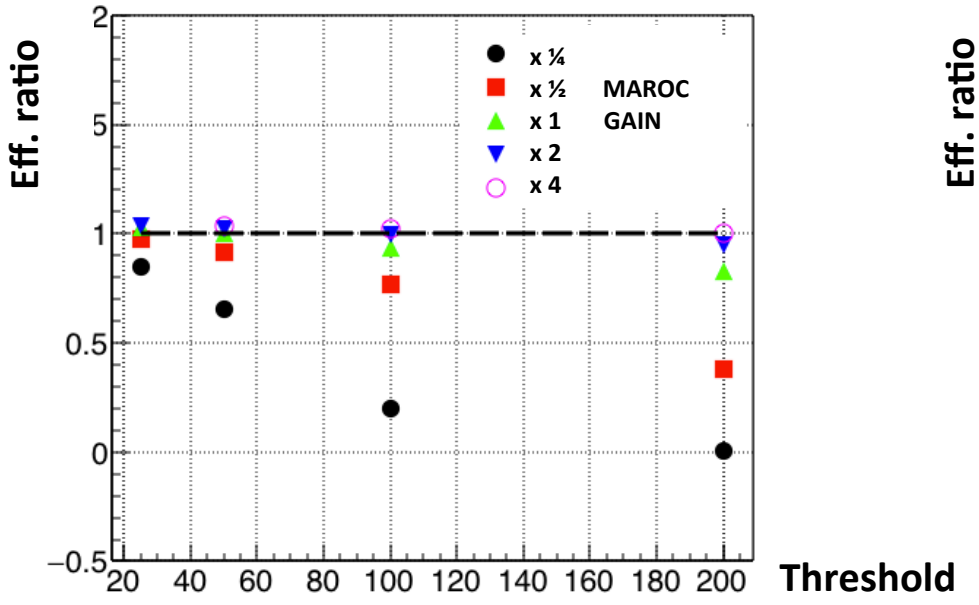
95	93	94	92	96	98	97	99
91	89	90	88	100	102	101	103
87	85	86	84	104	106	105	107
83	81	82	80	108	110	109	111
79	77	78	76	112	114	113	115
75	73	74	72	116	118	117	119
71	69	70	68	120	122	121	123
67	65	66	64	124	126	125	127

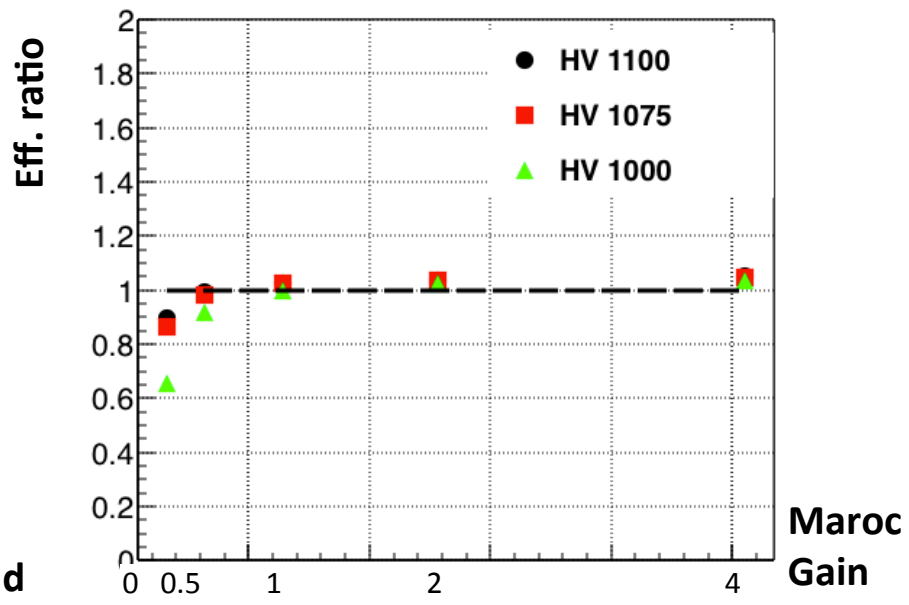


FE Electronics: SPE Discrimination



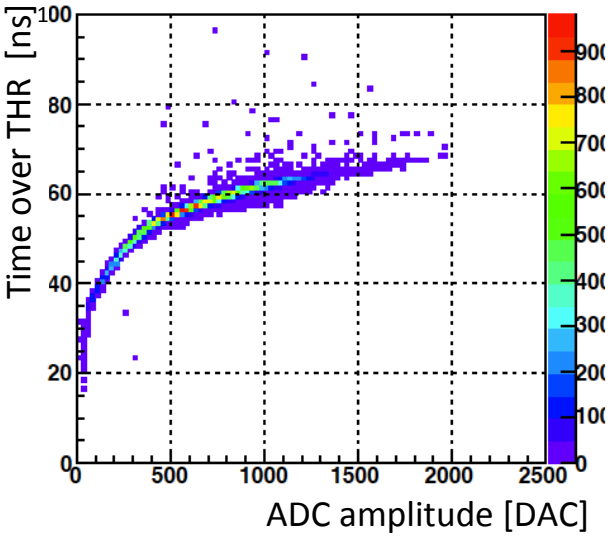




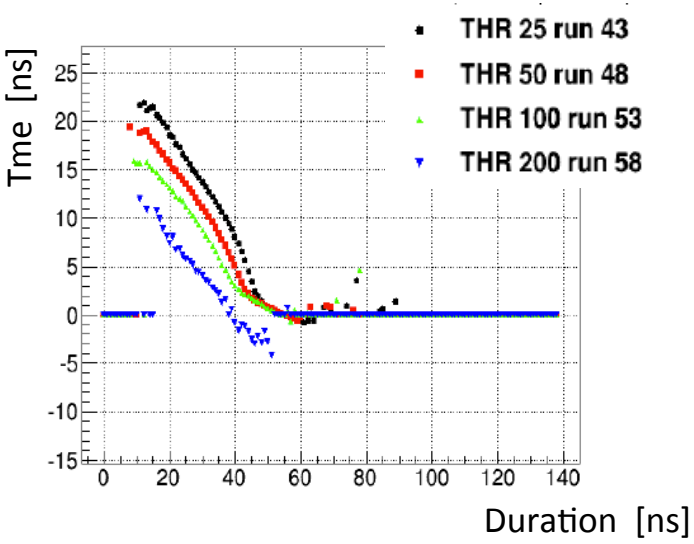


FE Electronics: SPE Timing

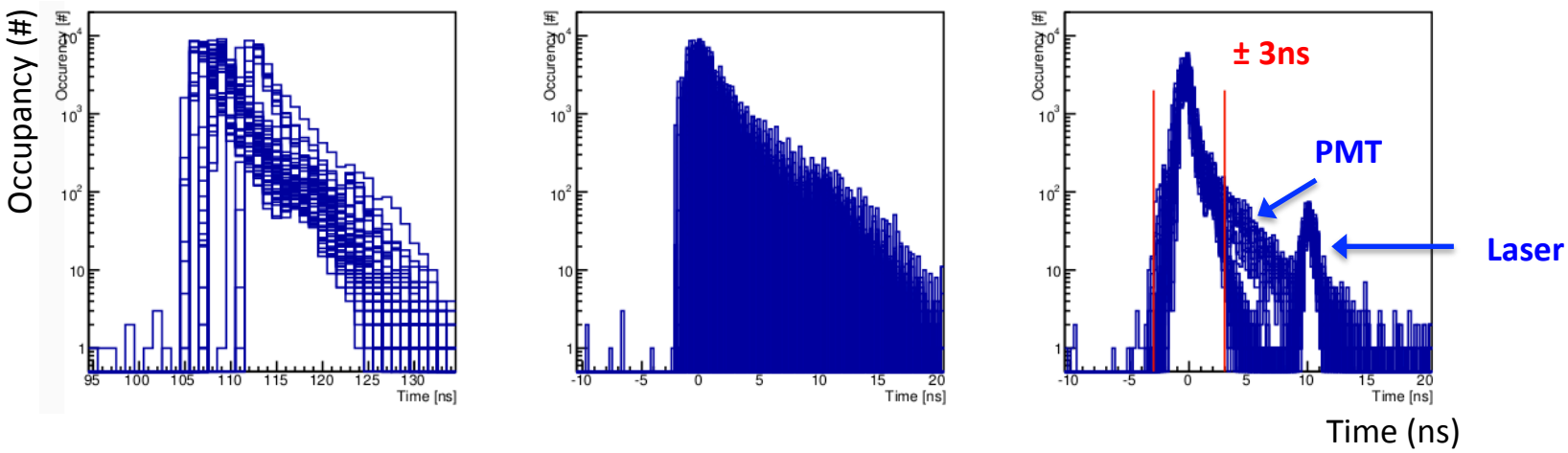
Time over threshold relates to charge



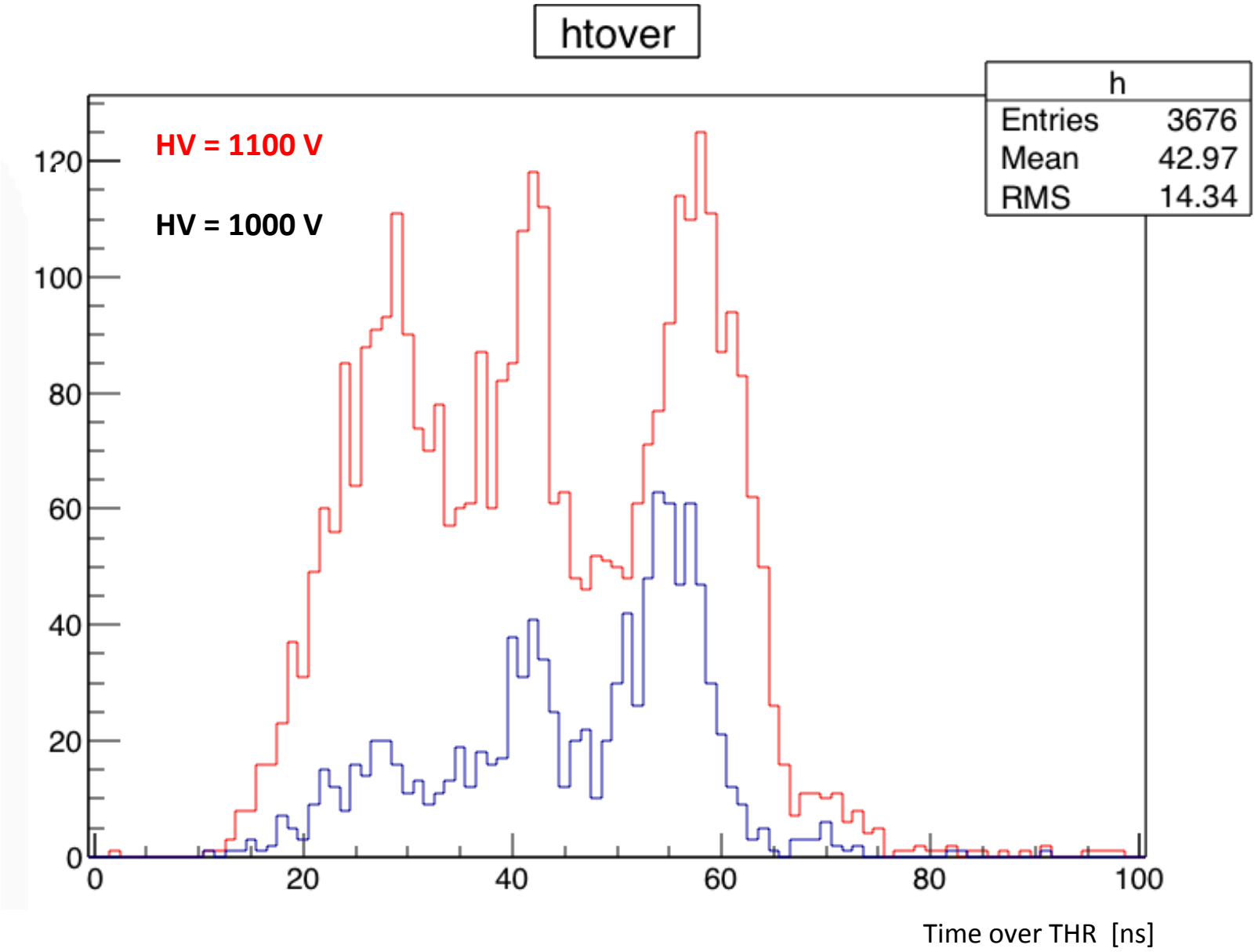
Typical time-walk with charge



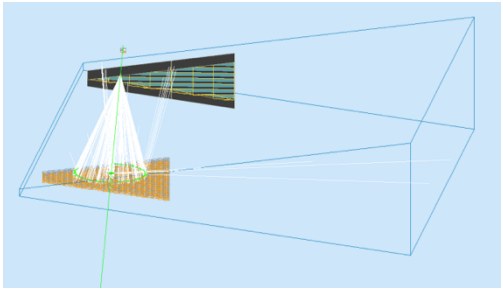
Channel by channel time calibration: -offsets -walk

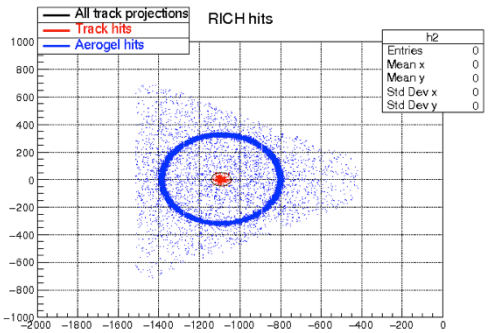


TDC Dark Counts



Cosmic Run

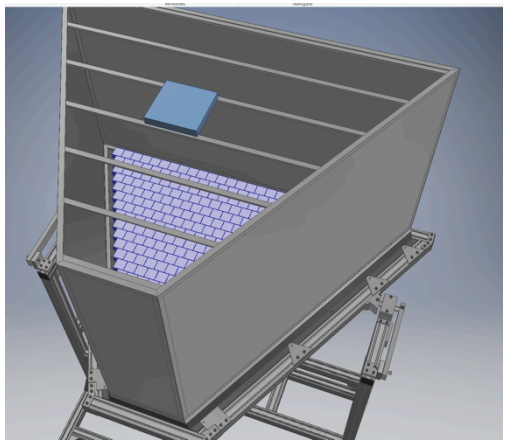




Phase 1 (June-July):

- fixed geometry
- 32 readout tiles (30 on the ring, 2 for tracking)
- SVT black cover

Goal: full readout chain



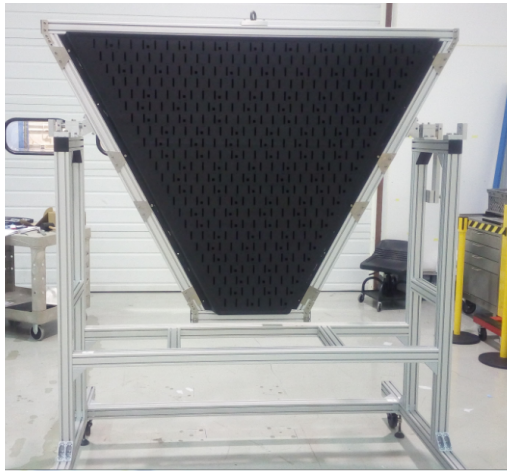
Phase 2 (August):

- Full panel instrumented
- Custom light-tight box
- Various track patterns

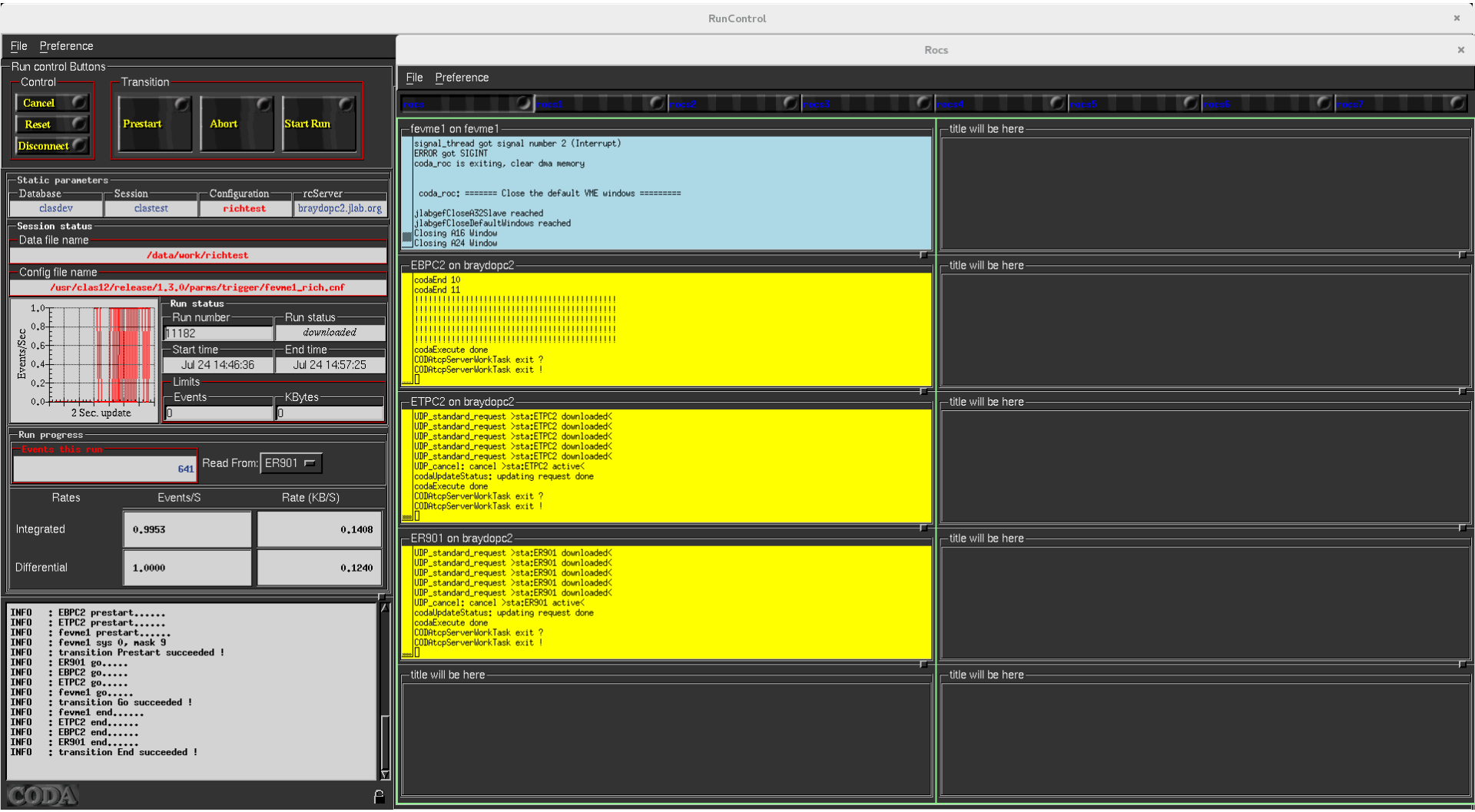
Goal: RICH readout commissioning

Important to define/commission

- space and time alignment
- photon vs track signals
- gemc simulations
- coat-java reconstruction
- monitor suite
  - slow control
  - event display
- calibration suite



SSP: CODA Control



SSP: Event Builder

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               0x2          0x81           0
   </bank>
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      </uint32>
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          c,i,l,N(c,c,s)
         </int8>
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            32bit: 0x00000002(2)                     Event number = 2
            64bit: 0x7615ea00014d(129836492259661)   48bit Timestamp = 0x00014d7615ea
          18(
            08bit: 0x00(uchar=0 char=0)
            08bit: 0x00(uchar=0 char=0)      Hit0    Fiber=0
            16bit: 0x003a(58)                        Channel=0
                                                     Edge=0,TDC=58
            08bit: 0x00(uchar=0 char=0)
            08bit: 0x00(uchar=0 char=0)      Hit1    Fiber=0
            16bit: 0xffff8070(-32656)                Channel=0
                                                     Edge=1,TDC=112
            08bit: 0x00(uchar=0 char=0)
            08bit: 0x40(uchar=64 char=64)    Hit2
            16bit: 0x0040(64)

            08bit: 0x00(uchar=0 char=0)
            08bit: 0x40(uchar=64 char=64)    Hit3
            16bit: 0xffff8075(-32651)

            08bit: 0x00(uchar=0 char=0)
            08bit: 0x80(uchar=128 char=-128) Hit4
            16bit: 0x003c(60)

            08bit: 0x00(uchar=0 char=0)
            08bit: 0x80(uchar=128 char=-128) Hit5
            16bit: 0xffff806f(-32657)
                                             <-- (...6 more hits for fiber 1 here - removed for this example)
            08bit: 0x02(uchar=2 char=2)
            08bit: 0x00(uchar=0 char=0)      Hit12
            16bit: 0x003c(60)

            08bit: 0x02(uchar=2 char=2)
            08bit: 0x00(uchar=0 char=0)
            16bit: 0xffff8071(-32655)

            08bit: 0x02(uchar=2 char=2)              Fiber=2
            08bit: 0x40(uchar=64 char=64)            Channel=64
            16bit: 0x0040(64)                        Edge=0,TDC=64

            08bit: 0x02(uchar=2 char=2)
            08bit: 0x40(uchar=64 char=64)
            16bit: 0xffff8073(-32653)

            08bit: 0x02(uchar=2 char=2)
            08bit: 0x80(uchar=128 char=-128)
            16bit: 0x0042(66)

            08bit: 0x02(uchar=2 char=2)
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ROC ID BANK: 84 = fevme1

TI BANK (0xe10a)

SSP RICH BANK (0xe124)