

RICH installation planned dates as agreeded with Bob Miller:

- August: LTCC sector #4 will be removed from the forward carriage
- September 11 (+1 week of contingency) :
air compressor, tank, control panel, crates and cables in Hall B
- September 16 (+1 week of contingency) : DSG starts cabling
- October 15 (+1 week of contingency) : RICH in Hall B

Latests

- Mechanics:** OSP for RICH component installation approved
Support structure installed: good fit to RICH
Several elements being 3D printed at JLab
Design ongoing of the installation brackets (last major item)
- Planar Mirrors:** All lateral mirrors done, shipment to JLab next week
Front mirrors under production. Shipment to JLab: 18th of September.
- Spherical Mirrors:** Dispatch from ECI to CMA starts today
Reflectivity of mirror#3 has been measured by DSG at Yuri's stand
5 spots: 85% - 90% reflectivity for wavelengths 430nm to 650nm
- Aerogel:** All 2 cm squared tiles ready for dispatch
8 tiles remaining to be shaped
- Electronics:** 40 F-E units characterized
All MAROC boards (except one) revised by R. Malaguti
Extended TDC tests under way
Cosmic stand installation initiated
SSP firmware pretty advanced (TDC event builder available)
- Software:** Monitor suite basically ready to play with SSP
Calibration challenge planned in August

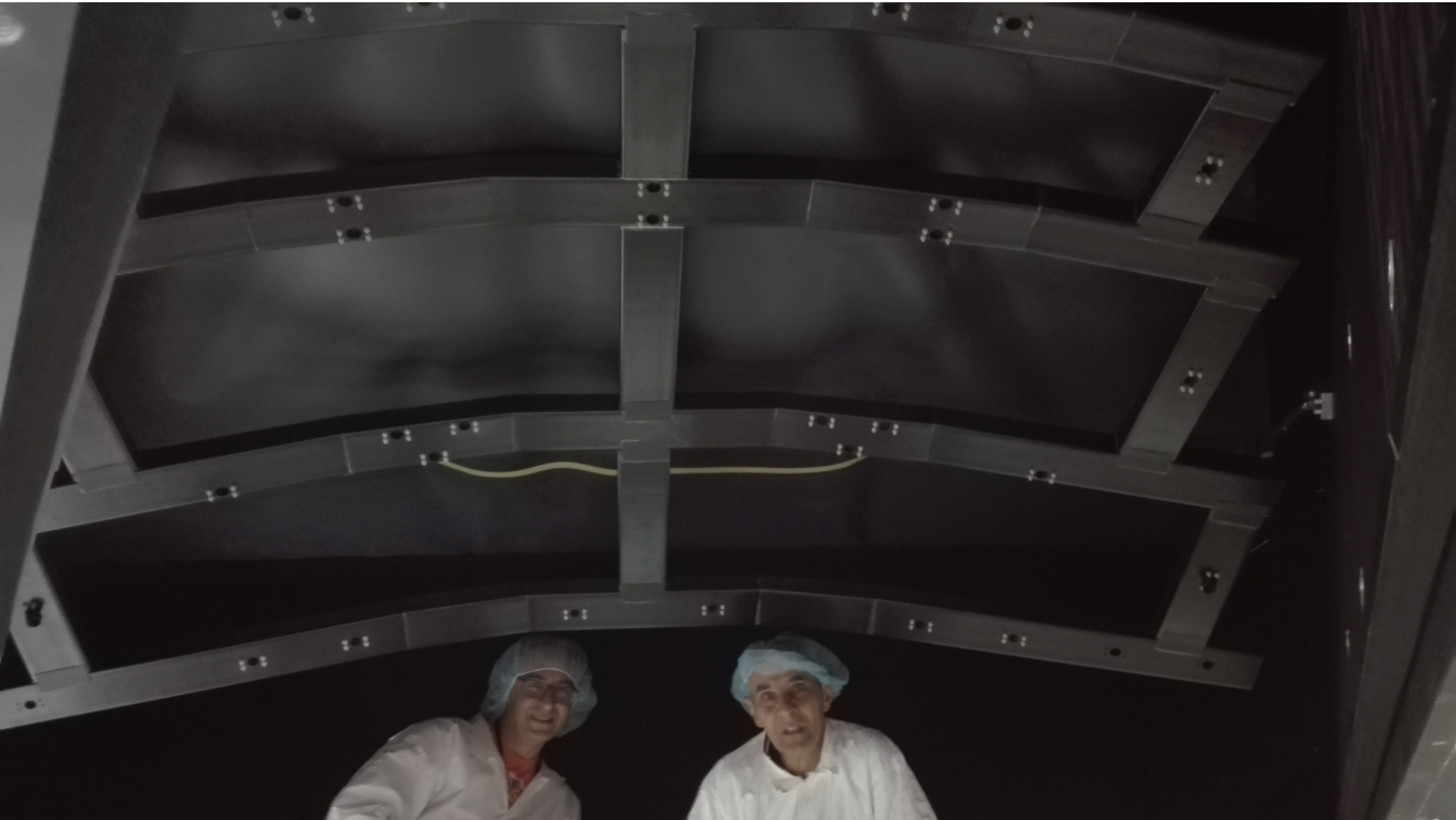
Mechanics

Electronic Panel



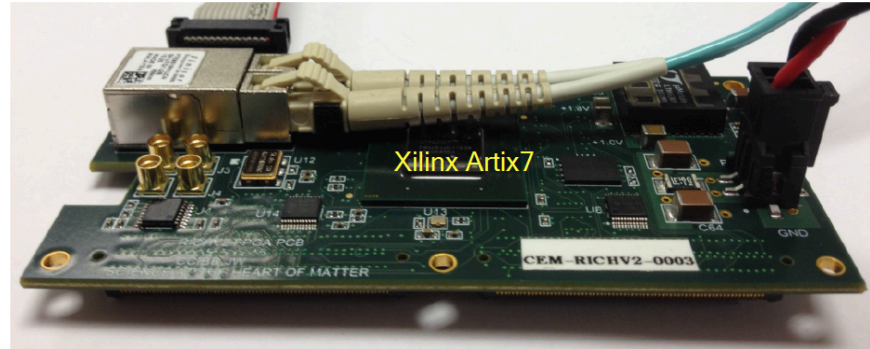
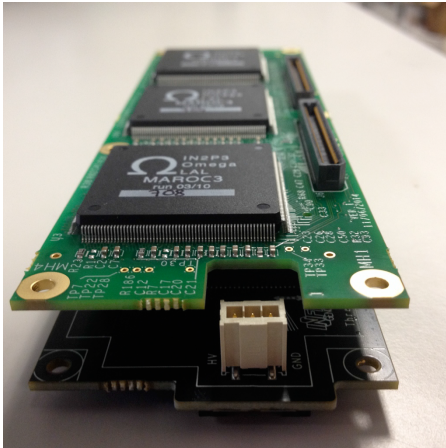
Mechanics

Spherical Mirror Support



RICH Front-End Electronics

In collaboration with FE group



example of MAROC signal processing

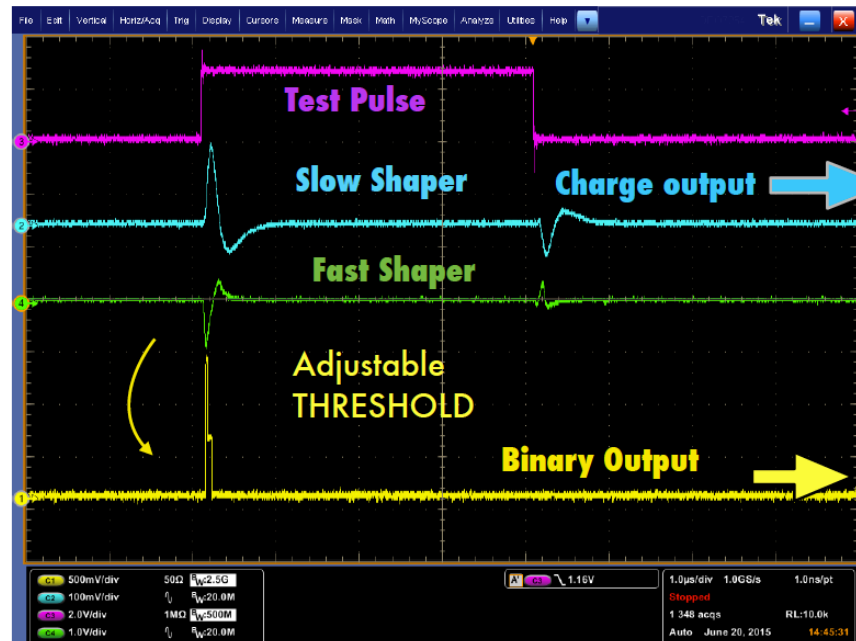
Analog: Charge (1 fC)
Digital: Time (1 ns)

Trigger latency (8 μ s)

Optical ethernet (2.5 Gbps)

Trigger: external
internal
self

On-board pulser



**ADC
(MAROC)**
calibration only
more on backup slide

**SCALER/TDC
(FPGA)**

**TDC used for
physics runs!**

Single channel response, 1 microsecond/div

Calibration

- ✗ Multiplexed ADC charge measurement **LINEAR but only meant as a calibration tool**

Can not be used during CLAS12 data-taking (not enough trigger latency, fixed time delay vs TRG)

Parameters as **gain, relative and absolute efficiency** from LaserTED are useful to validate TDC

Gain = SPE model value fitted from charge spectrum

Relative Eff = Charge spectrum integral above threshold / SPE model integral

Absolute Eff = # events with charge above threshold / # triggers
(assumes uniform laser light illumination)

Necessary to deal with cross-talk (optics and electronics) to avoid over-estimate

- ✗ Parallel TDC digital readout: **NOT-LINEAR but charge estimation**

Gain = estimate from time-over-THR spectrum



Required to monitor stability in time

Relative Eff = only possible in comparison to ADC, or to a lower THR

Absolute Eff = # events with charge above threshold / # triggers
(assumes uniform laser light illumination)



Required for Likelihood

Time = 1ns timestamp provided by FPGA

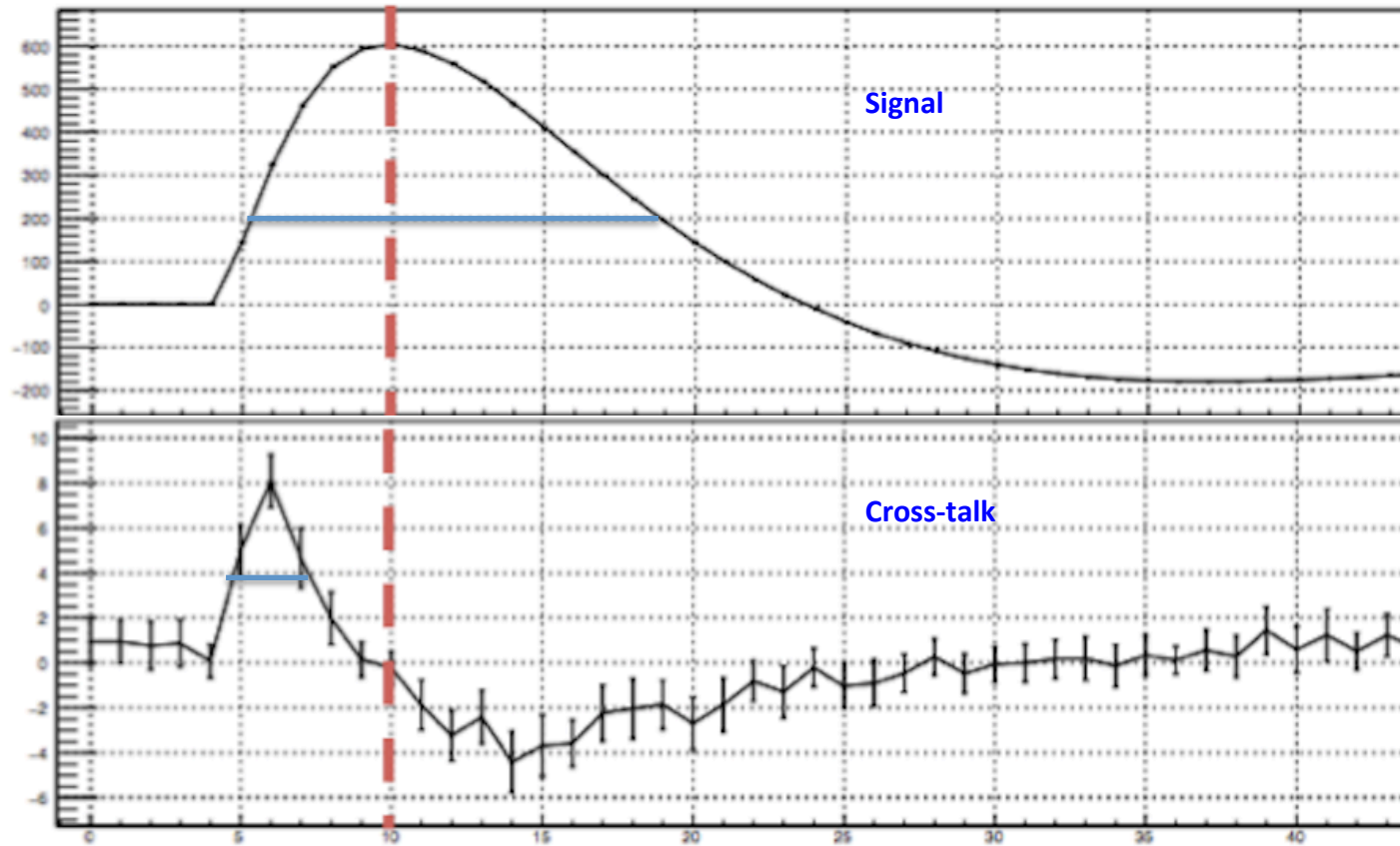


Required for Likelihood

Calibration

ADC

TDC



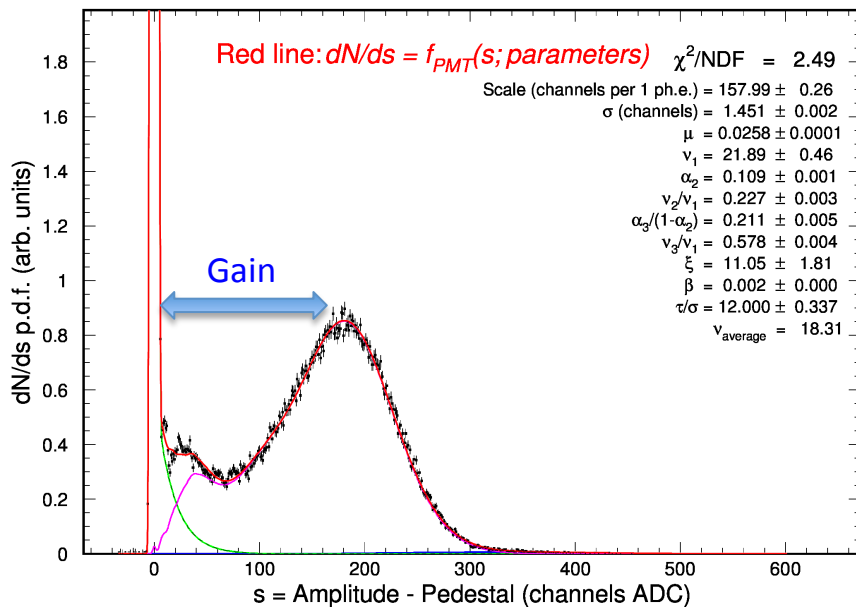
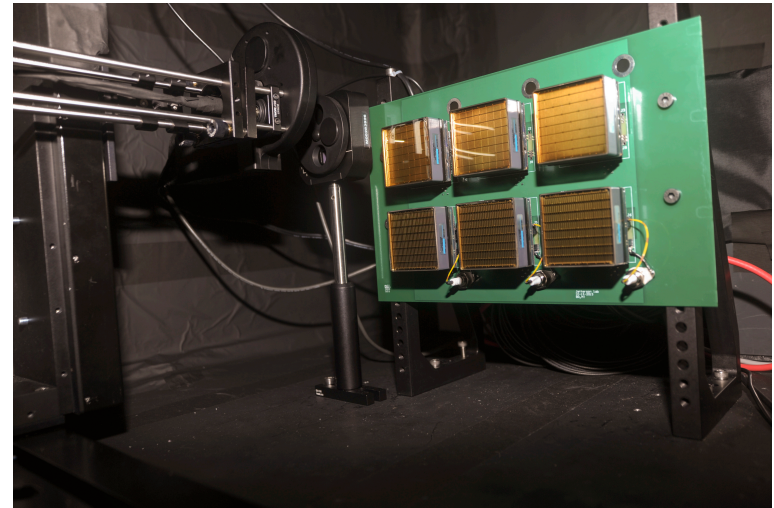
FE Electronics: Charge

Multiplexed readout up to 50 kHz

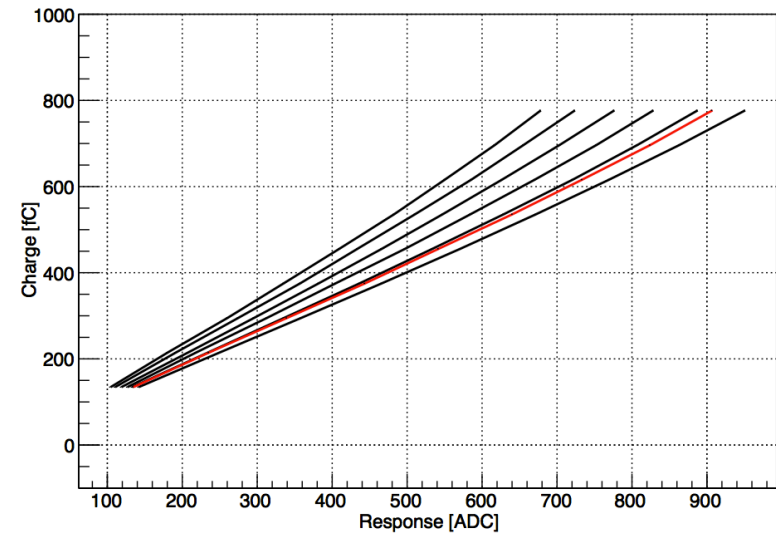
High resolution SPE spectrum

Viable for **efficiency** and **gain** monitors

In conjunction with timing, allows the study of PMT discharge and cross-talk



ADC Calibration (Slow Shaper)



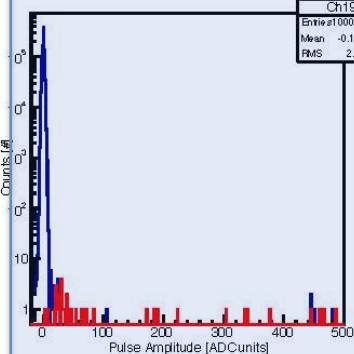
RICH Electronic: Cross-talk

GA0501

95	93	94	92	96	98	97	99
91	89	90	88	100	102	101	103
87	85	86	84	104	106	105	107
83	81	82	80	108	110	109	111
79	77	78	76	112	114	113	115
75	73	74	72	116	118	117	119
71	69	70	68	120	122	121	123
67	65	66	64	124	126	125	127

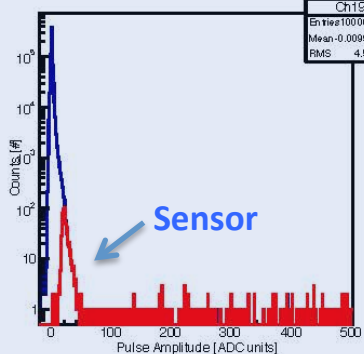
ASIC 1 CHANNEL 27 CHTILE 91

Ch191
Entries: 1000006
Mean: -0.1723
RMS: 2.317



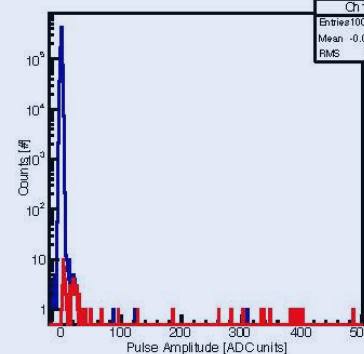
ASIC 1 CHANNEL 25 CHTILE 89

Ch191
Entries: 1000006
Mean: -0.009904
RMS: 4.536



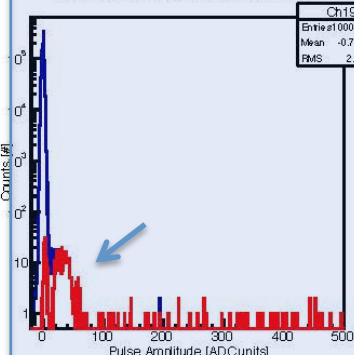
ASIC 1 CHANNEL 26 CHTILE 90

Ch191
Entries: 1000006
Mean: -0.08976
RMS: 1.942



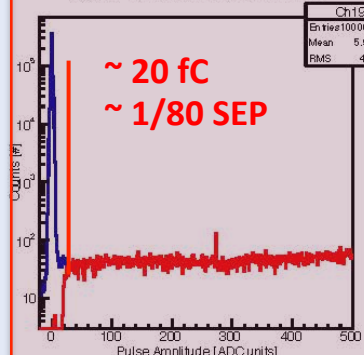
ASIC 1 CHANNEL 23 CHTILE 87

Ch191
Entries: 1000006
Mean: -0.7392
RMS: 2.974



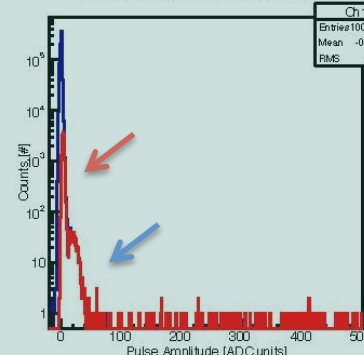
ASIC 1 CHANNEL 21 CHTILE 85

Ch191
Entries: 1000006
Mean: 5.946
RMS: 45.8



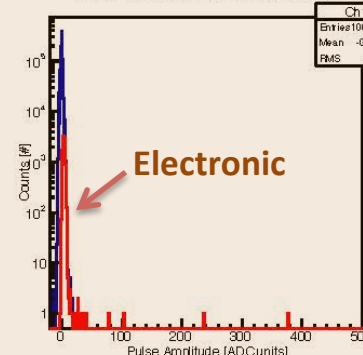
ASIC 1 CHANNEL 22 CHTILE 86

Ch191
Entries: 1000006
Mean: -0.6405
RMS: 3.543



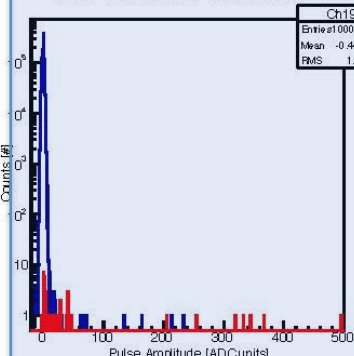
ASIC 1 CHANNEL 20 CHTILE 84

Ch191
Entries: 1000006
Mean: -0.4765
RMS: 1.608



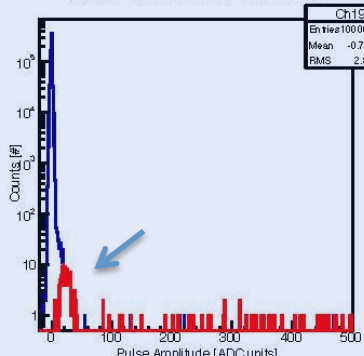
ASIC 1 CHANNEL 19 CHTILE 83

Ch191
Entries: 1000006
Mean: -0.4407
RMS: 1.876



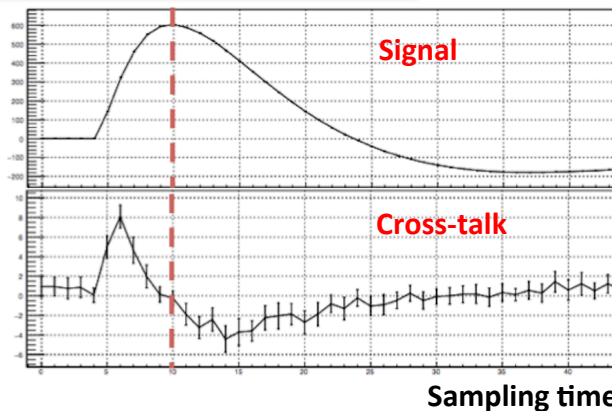
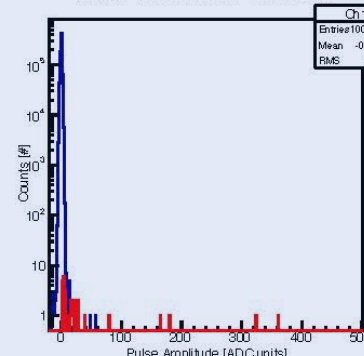
ASIC 1 CHANNEL 17 CHTILE 81

Ch191
Entries: 1000006
Mean: -0.7921
RMS: 2.859



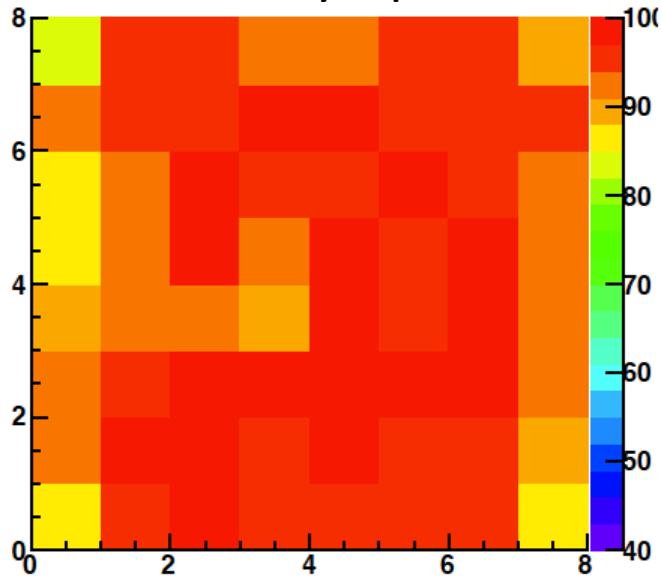
ASIC 1 CHANNEL 18 CHTILE 82

Ch191
Entries: 1000006
Mean: -0.2393
RMS: 1.508

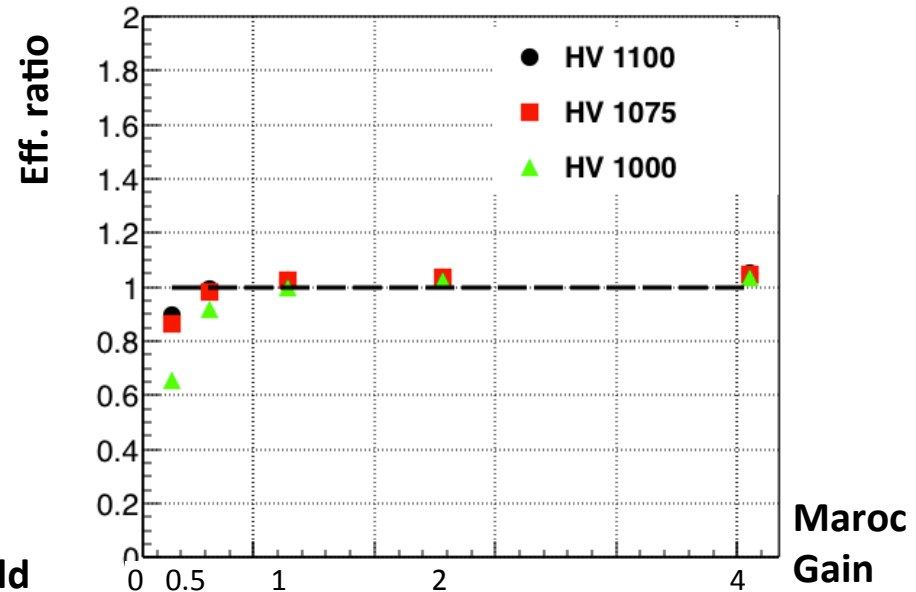
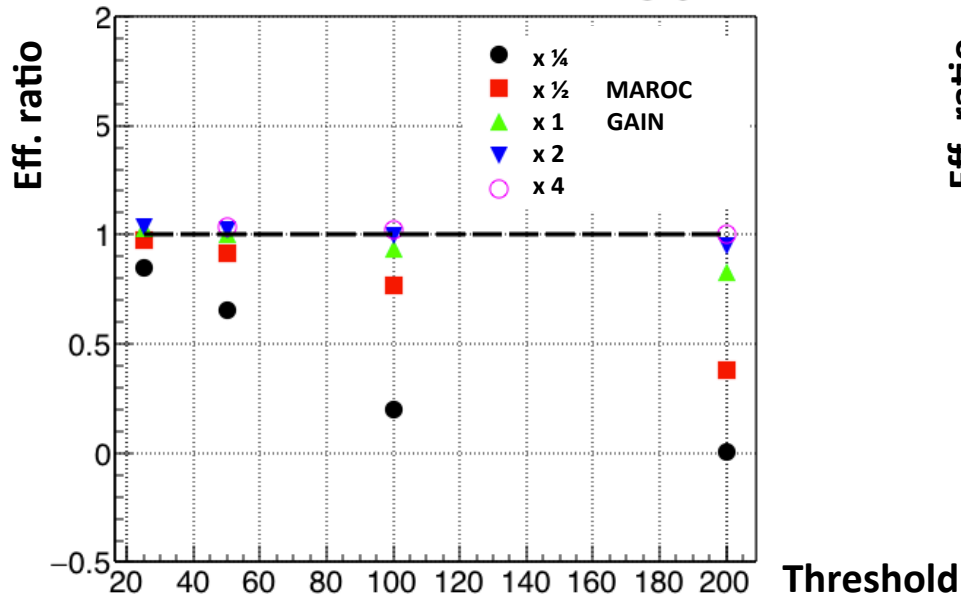
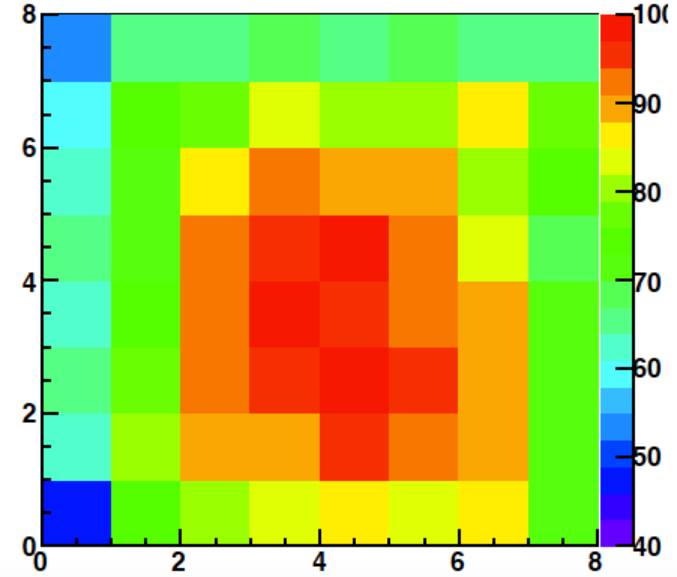


FE Electronics: SPE Discrimination

Relative efficiency map

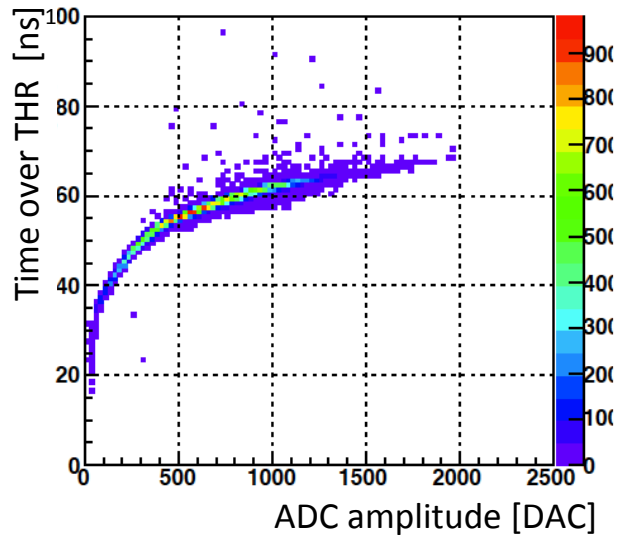


Relative gain map

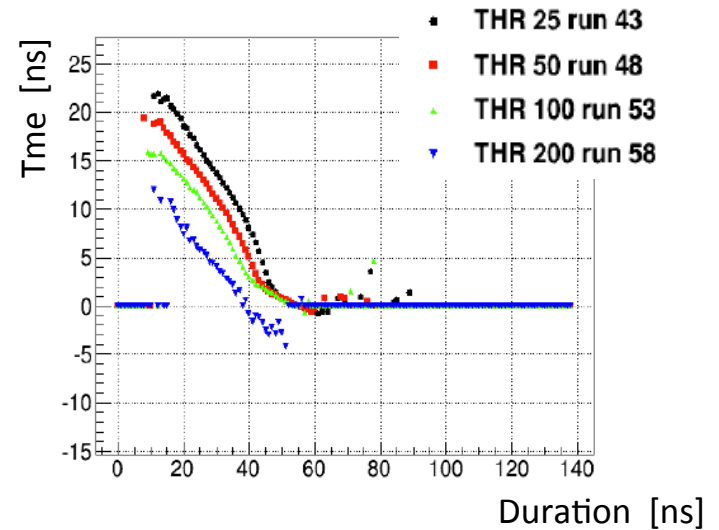


FE Electronics: SPE Timing

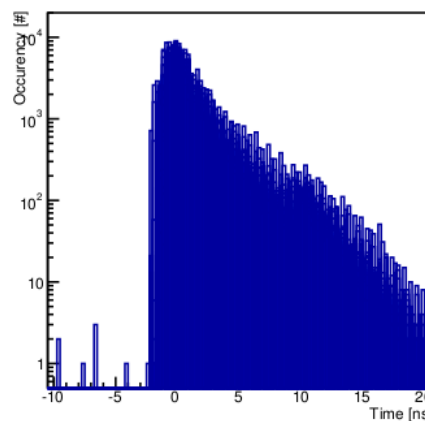
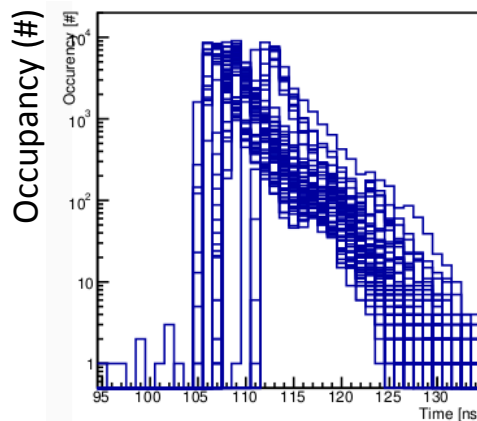
Time over threshold relates to charge



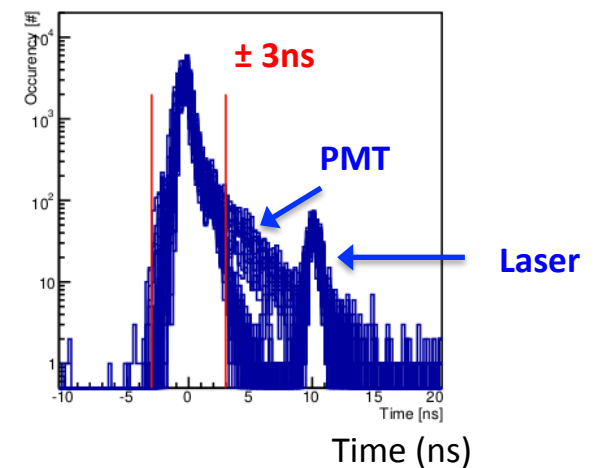
Typical time-walk with charge



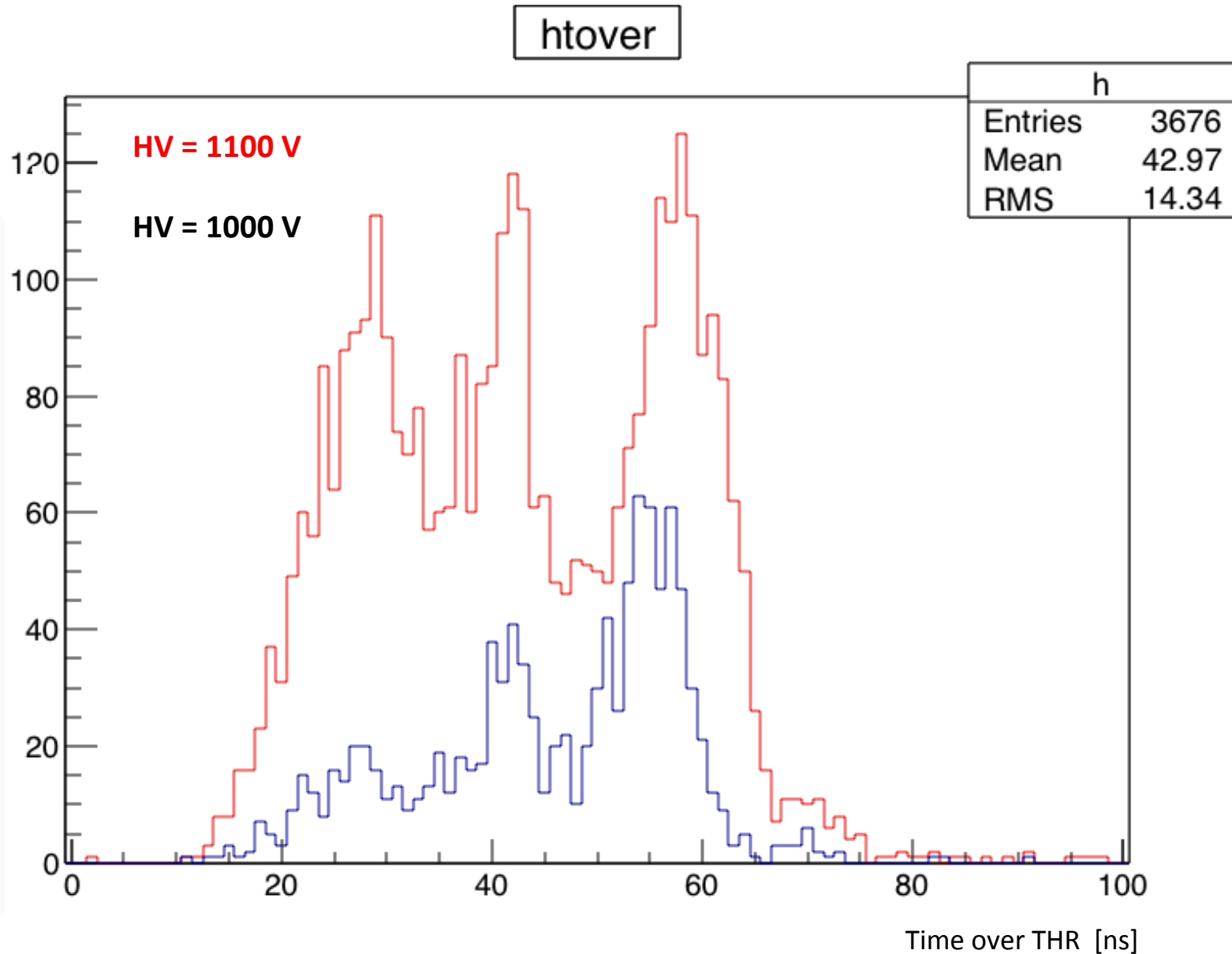
Channel by channel time calibration: -offsets



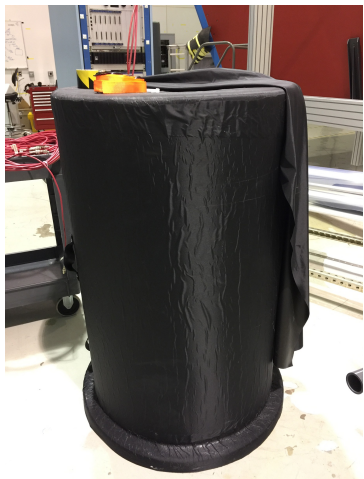
-walk



TDC Dark Counts



Cosmic Run



Phase 1 (June-July):

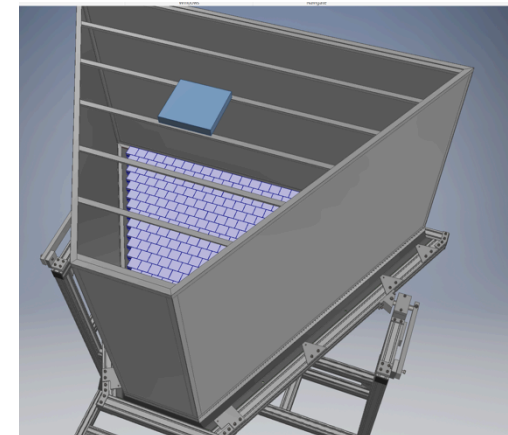
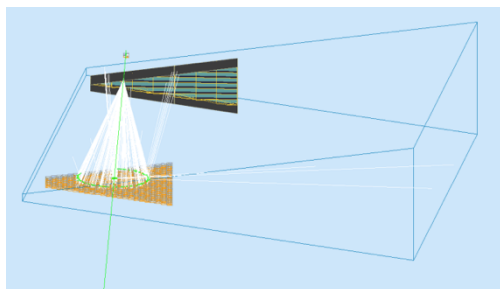
- fixed geometry
- 32 readout tiles (30 on the ring, 2 for tracking)
- SVT black cover

Goal: full readout chain

Phase 2 (August):

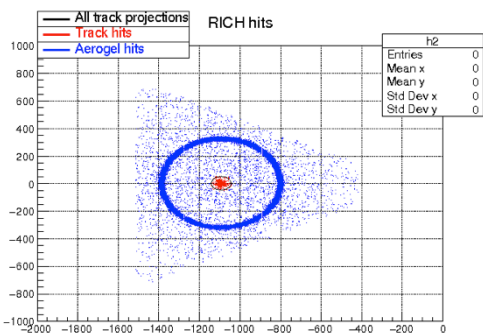
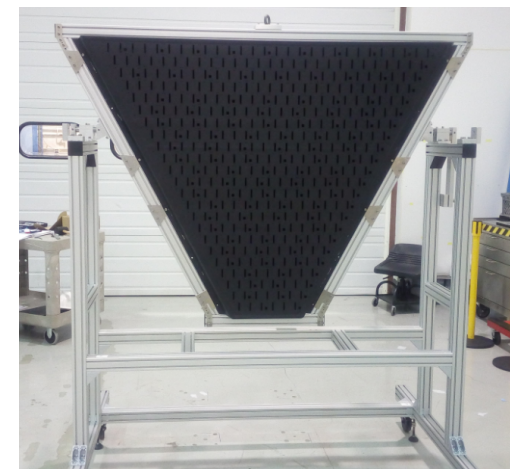
- Full panel instrumented
- Custom light-tight box
- Various track patterns

Goal: RICH readout commissioning



Important to define/commission

- space and time alignment
- photon vs track signals
- gemc simulations
- coat-java reconstruction
- monitor suite
 - slow control
 - event display
- calibration suite



SSP: CODA Control

The screenshot displays the RunControl application interface, which is used for managing and monitoring the execution of SSP (System Support Program) tasks. The interface is divided into several functional areas:

- Run control Buttons:** Located at the top left, it includes a 'Control' section with 'Cancel', 'Reset', and 'Disconnect' buttons, and a 'Transition' section with 'Prestart', 'Abort', and 'Start Run' buttons. The 'Start Run' button is highlighted with a red box.
- Static parameters:** A table below the buttons showing configuration details:

Database	Session	Configuration	rcServer
clasdev	clastest	richest	braydopc2.jlab.org
- Session status:** Shows the current data file name as '/data/work/richest' and the config file name as '/usr/clas12/release/1.3.0/parms/trigger/fevnel_rich.cnf'. A graph below shows 'Events/Sec' over time, with a 2-second update interval.
- Run progress:** Displays 'Events this run' as 641 and 'Read From' as ER901.
- Rates:** A table showing performance metrics:

	Events/S	Rate (KB/S)
Integrated	0.9953	0.1408
Differential	1.0000	0.1240
- Terminal Window:** The main area on the right, titled 'Rocs', contains a multi-pane terminal. The top pane shows error messages: 'signal_thread got signal number 2 (Interrupt)', 'ERROR: got SIGINT', and 'codaroc is exiting, clear dma memory'. The middle pane shows 'EBPC2 on braydopc2' with a yellow background and a progress indicator. The bottom pane shows 'ETPC2 on braydopc2' and 'ER901 on braydopc2' with similar yellow backgrounds and progress indicators. The right side of the terminal window contains several 'title will be here' placeholders.

SSP: Event Builder

```
2
3 -event format="evio" count="4" content="bank" data_type="0x10" tag="129(0x0081)" padding="0" num="204" length="55" ndata="53">
4 -bank content="uint32" data_type="0x1" tag="49152(0xc000)" padding="0" num="0" length="5" ndata="3">
5   0x2          0x81          0
6 </bank>
7 -bank content="bank" data_type="0xe" tag="84(0x0054)" padding="0" num="2" length="48" ndata="46"> ROC ID BANK: 84 = fevme1
8 -uint32 data_type="0x1" tag="57610(0xe10a)" padding="0" num="0" length="7" ndata="5"> TI BANK (0xe10a)
9   0x1010004    0x2      0x9aec428d    0x16e00002    0xda560001
10 </uint32>
11 <-composite data_type="0xf" tag="57636(0xe124)" padding="0" num="0" length="32" ndata="30"> SSP RICH BANK (0xe124)
12   <-int8 data_type="0x6" tag="14(0x000e)">
13     c,i,l,N(c,c,s)
14   </int8>
15   <-data>
16     <-row>
17       08bit: 0x08(uchar=8 char=8)          SSP VME Slot = 8
18       32bit: 0x00000002(2)                Event number = 2
19       64bit: 0x7615ea00014d(129836492259661) 48bit Timestamp = 0x00014d7615ea
20     18(
21       08bit: 0x00(uchar=0 char=0)          Hit0      Fiber=0
22       08bit: 0x00(uchar=0 char=0)          Channel=0
23       16bit: 0x003a(58)                    Edge=0,TD C=58
24
25       08bit: 0x00(uchar=0 char=0)          Hit1      Fiber=0
26       08bit: 0x00(uchar=0 char=0)          Channel=0
27       16bit: 0xffff8070(-32656)           Edge=1,TD C=112
28
29       08bit: 0x00(uchar=0 char=0)          Hit2
30       08bit: 0x40(uchar=64 char=64)
31       16bit: 0x0040(64)
32
33       08bit: 0x00(uchar=0 char=0)          Hit3
34       08bit: 0x40(uchar=64 char=64)
35       16bit: 0xffff8075(-32651)
36
37       08bit: 0x00(uchar=0 char=0)
38       08bit: 0x80(uchar=128 char=-128) Hit4
39       16bit: 0x003c(60)
40
41       08bit: 0x00(uchar=0 char=0)
42       08bit: 0x80(uchar=128 char=-128) Hit5
43       16bit: 0xffff806f(-32657)
44     (...6 more hits for fiber 1 here - removed for this example)
45     08bit: 0x02(uchar=2 char=2)          Hit12
46     08bit: 0x00(uchar=0 char=0)
47     16bit: 0x003c(60)
48
49     08bit: 0x02(uchar=2 char=2)
50     08bit: 0x00(uchar=0 char=0)
51     16bit: 0xffff8071(-32655)
52
53     08bit: 0x02(uchar=2 char=2)          Fiber=2
54     08bit: 0x40(uchar=64 char=64)        Channel=64
55     16bit: 0x0040(64)                    Edge=0,TD C=64
56
57     08bit: 0x02(uchar=2 char=2)
58     08bit: 0x40(uchar=64 char=64)
59     16bit: 0xffff8073(-32653)
60
61     08bit: 0x02(uchar=2 char=2)
62     08bit: 0x80(uchar=128 char=-128)
63     16bit: 0x0042(66)
64
65     08bit: 0x02(uchar=2 char=2)
66     08bit: 0x80(uchar=128 char=-128)
67     16bit: 0xffff8077(-32649)
68   </row>
69   </data>
70 </composite>
71 -uint32 data_type="0x1" tag="57615(0xe10f)" padding="0" num="0" length="7" ndata="5">
72   0          0x2bbb          0x2      0x59775fa5          0x1
73 </uint32>
74 </bank>
75 </event>
76
77 <!-- end buffer 4 -->
78
```