

## RICH Detector Status

M. Contalbrigo INFN Ferrara

Hall-B Meeting 11 September 2017

## CLAS12 RICH



# INSTITUTIONSINFN (Italy)Bari, Ferrara, Genova, L.Frascati, Roma/ISSJefferson Lab (Newport News, USA)Argonne National Lab (Argonne, USA)Duquesne University (Pittsburgh, USA)George Washington University (USA)Glasgow University (Glasgow, UK)Kyungpook National University, (Daegu, Korea)University of Connecticut (Storrs, USA)UTFSM (Valparaiso, Chile)



#### **Prototype results:**

# **RICH** Design

Goal: separate kaons from pions and protons in the momentum range 3-8 GeV/c

Aerogel radiator to match the momentum Hybrid-optic to minimize the instrumented area Working with VIS and near-UV photons (MAPMTs or SiPMs)



# **Mechanic Assembling**

- External RICH vessel assembled in EEL-124
- Entrance, exit and electronic panels ready
- Assembling tools ready

## Entrance bottom



Entrance top



## Thanks to DSG group!

## **Electronic Panel**



Aerogel

✓ 3 cm: minimal quantity @ JLab



2 cm: all squared tiles @ JLab
 2 cm corner tiles ready for shipment



additional spares being produced

#### Most critical parameter: scattering length



## **Spherical Mirrors**



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## **Planar Mirrors**

- Lateral mirror @ JLab
  Material budget comparable to CFRP @ 1/10 cost
- Assembling validated
- Surface defects mitigated
- Front mirror production ongoing (done next week)

#### Front panel and mirror assembling test



Reflectivity specs: > 90% at 400 nm



#### Slope of surface from CMM machine



## **RICH Readout Electronics**

## **Services** SSP Fiber-Optic DAQ **Readout Electronics Air Cooling** Compact (matches sensor area) Modular Front-End (Mechanical adapter, ASIC, FPGA) Scalable fiber optic DAQ (TCP/IP or SSP) Tessellated (common HV, LV and optical fiber) ADAPTER BOARD PMTs ASIC BOARD FPGA BOARD **Electronic Panel**

## **RICH Front-End Electronics**



Analog: Charge (1 fC) Digital: Time (1 ns)

Trigger latency (8 µs)

Optical ethernet (2.5 Gbps)

Trigger: external internal self

On-board pulser



example of MAROC signal processing



Single channel response, 1 microsecond/div

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## **ADC: Collected Charge**

## MAPMT model for gain, resolution, SPE efficiency accounting for cross--talk









#### SPE relative efficiency: +20% for H12700



## **TDC: SPE Discrimination Calibration**



# **TDC: SPE Timing Calibration**

#### Time over threshold relates to charge



#### Typical time-walk with charge



#### Channel by channel time calibration: -o











## **Cosmic Stand**



## Cosmic Run



Trigger and tracking station





#### Scintillator pads



# **Power Supply Control**

🌃 HVRICH1 - Board #11 🖾

## LV voltages

### **HV Voltages**

🞽 HVI	RICH1 - Board #00 없								
Cor	ntrols HVRI	CH1 E	Board	#00					
#	Description	Pw	∨mon	Imon	Status	∨set (∨)	lset (uA)		
00	HVRICH1_LV_SPARE_SI00_Ch	00 <b>ON</b>	5.19 V	3.07 A	ON	5.200 ∨	4.0 A	]	
01	HVRICH1_LV_SPARE_SI00_Ch	01 <b>ON</b> )	5.20 V	3.10 A	ON	5.200 V	4.0 A	1	
02	HVRICH1_LV_SPARE_SI00_Ch	02 <b>ON</b>	5.20 V	3.12 A	ON	5.200 V	4.0 A	1	
03	HVRICH1_LV_SPARE_SI00_Ch	03 <b>ON</b>	5.20 V	3.13 A	ON	5.200 V	4.0 A	1	
04	HVRICH1_LV_SPARE_SI00_Ch	04 <b>ON</b>	5.20 V	3.11 A	ON	5.200 V	4.0 A	1	
05	HVRICH1_LV_SPARE_SI00_Ch	05 <b>ON</b>	5.20 V	3.10 A	ON	5.200 V	4.0 A	1	
06	HVRICH1_LV_SPARE_SI00_Ch	06 <b>ON</b>	5.20 V	3.12 A	ON	5.200 V	4.0 A	1	
07	HVRICH1_LV_SPARE_SI00_Ch	07 <b>ON</b>	5.20 V	3.10 A	ON	5.200 V	4.0 A		



Con		11 E	Board	#11			
#	Description	Pw	Vmon	Imon	Status	Vset (V)	lset (uA)
00	HVRICH1_HV_SPARE_SI11_Ch00		0.00 V	0.00 uA	OFF	0.000 V	100.0 uA
01	HVRICH1_HV_SPARE_SI11_Ch01	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
02	HVRICH1_HV_SPARE_SI11_Ch02	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
03	HVRICH1_HV_SPARE_SI11_Ch03	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
04	HVRICH1_HV_SPARE_SI11_Ch04	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
05	HVRICH1_HV_SPARE_SI11_Ch05	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
06	HVRICH1_HV_SPARE_SI11_Ch06	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
07	HVRICH1_HV_SPARE_SI11_Ch07	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
08	HVRICH1_HV_SPARE_SI11_Ch08	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
09	HVRICH1_HV_SPARE_SI11_Ch09	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
10	HVRICH1_HV_SPARE_SI11_Ch10	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
11	HVRICH1_HV_SPARE_SI11_Ch11	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
12	HVRICH1_HV_SPARE_SI11_Ch12	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
13	HVRICH1_HV_SPARE_SI11_Ch13	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
14	HVRICH1_HV_SPARE_SI11_Ch14	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
15	HVRICH1_HV_SPARE_SI11_Ch15	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
16	HVRICH1_HV_SPARE_SI11_Ch16		1300.02 V	698.49 uA	ON	1300.000 V	1550.0 uA
17	HVRICH1_HV_SPARE_SI11_Ch17		1299.98 V	698.47 uA	ON	1300.000 V	1550.0 uA
18	HVRICH1_HV_SPARE_SI11_Ch18	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
19	HVRICH1_HV_SPARE_SI11_Ch19		0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
20	HVRICH1_HV_SPARE_SI11_Ch20		0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
21	HVRICH1_HV_SPARE_SI11_Ch21		0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
22	HVRICH1_HV_SPARE_SI11_Ch22		0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
23	HVRICH1_HV_SPARE_SI11_Ch23		0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
24	HVRICH1_HV_SPARE_SI11_Ch24		0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
25	HVRICH1_HV_SPARE_SI11_Ch25	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
26	HVRICH1_HV_SPARE_SI11_Ch26	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
27	HVRICH1_HV_SPARE_SI11_Ch27	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
28	HVRICH1_HV_SPARE_SI11_Ch28	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
29	HVRICH1_HV_SPARE_SI11_Ch29	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
30	HVRICH1_HV_SPARE_SI11_Ch30	OFF	0.00 V	0.00 uA	OFF	0.000 V	155.0 uA
31	HVRICH1 HV SPARE SI11 Ch31	OFF	0.00 V	0.00 uA	OFF	0 000 V	155.0 uA

- 0

## **Slow Control**

#### 💒 RICH SSP Boards 🖾

Slot 3 Slot 4 Slot 5 Slot 6 Slot 7

Pmt 0

44

26

2050549

24

25

28

25

12

Scaler Average (Hz)

Pmt 1

17

27

26

15

52

10

14

26

122

Pmt 2

11

46

22

40

38

11

12

FPGA

43.97

44.53

43.91

43.61

43.20

41.57

38.60

43.56

41.55

Menu

Fiber

00

01

02

03

04

05

06

07

08

09

10

Slot

04

04

04

04

04

04

04

04

04

04

04

04 04 04 04 04	12 13 14 15	Scaler for eac	Averag ch PMT	e (Hz)	Temp each	peratur FE unit	es for (C)		B	ias volt ach FE	ages fo unit (V)	r	
04	16	28	22	17	42.49	37.34	37.36	5.004	3.336	0.992	1.786	0.996	1.199
04	17	19	12	12	40.03	33.05	35.72	5.029	3.343	0.996	1.789	1.000	1.198
04	18	13	7	6	41.23	35.62	37.78	5.033	3.327	0.991	1.782	0.997	1.194
04	19	25	23	414	40.03	35.99	36.40	5.026	3.327	0.992	1.786	0.996	1.195
04	20	10	20	49	43.92	39.19	39.48	5.029	3.346	0.993	1.783	0.996	1.197
04	21	24	29	10	40.65	37.21	33.28	5.027	3.339	0.994	1.787	0.999	1.196
04	22	10	7	49	40.60	35.60	36.03	5.022	3.339	0.991	1.780	0.998	1.192
04	23	10	5	41	42.44	36.08	33.35	5.045	3.327	0.993	1.786	1.000	1.200
04	24	12	10	6	39.61	35.54	36.81	5.036	3.343	0.995	1.787	0.994	1.195

Option: add some of these values to the interlock of the system

E

# **RICH Online Display**

Temperatures and Scalers monitored with warning signs





## Hardware Interlock

🎬 RICH-hwintlk.opi 🖾

## **RICH Hardware Interlock System User Interface**



31

Humidity 11

- -

## Mya Strip Charts

## Cosmic stand worked smoothly during first run (3 days)



## No background suppression: 1 microsec readout window



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Event #15291								
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## **Hit Time Distribution**

## $\Delta T$ (BOTTOM plane – TOP Tracking Unit) = 3.4 ns

 $\sigma_{T}$  without any correction = 2.4 ns



# **RICH Software**



RICH geometry is implemented in the software mostly from CAD through mesh files

- a detailed, consistent and updated description of the detector can be obtained
- simulation and reconstruction shared the same database

Digitization of the MAPMT response:

- calculate the pixel ID
- interface to CCDB
- apply efficiency
- simulated ADC and TDC spectra







Event reconstruction started

- match with DC information in coat-java
- photon tracing algorithm (tested with prototype and cosmic runs)
- event display

Strong crew: Matteo, Ilaria, Marco, Giovanni, Justin, Morgen, Elise, Aram, Andrey, ...

## **Photon Detector**

#### Scale the system up:

- Argonne cosmic box
- Cabling with patch panels
- ✓ Gas system being installed in EEL-124 (DSG)

Operative test foreseen in October 17 with fully instrumented electronic panel

#### Gas System GUI









Air Tank and Gas Line Controls Clean Air Compressor



## **Assembling Schedule**

						W	EK					
activity	aug 28	sep 4	sep 11	sep 18	sep 25	oct 2	oct 9	oct 16	oct 23	oct 30	nov 6	nov 13
EPanel tests with 32 boards												
Spherical mirror resurfacing and coating												
Aerogel production and delivery												
3D print of the pushers of the 2 cm layer												
Purchase of the wire and spacers												
Construction of the brackets for the load test												
Construction of the brackets for the strong-back												
Construction of the mounts for the trolley												
Setup of the gas slow control and interlocks												
3D print of the cooling distributor (left)												
Setup of the N2 dewar												
3D print of the N2 manyfold												
Cosmics box at JLab												
Production of the patch panels												
Assembly of the frontal panel tools												
Test of the lateral mirror installation												
Test of the prototype mirror B1 installation												
Production of fake tiles												
Setup of the dry area with the Fe cabinet												
Assembly test of the frontal panels												
Preliminary test of the cooling distributor												

September:

## Photon Detector Assembling

## **RICH Components Preparation**

						w	EEK					
activity	aug 28	sep 4	sep 11	sep 18	sep 25	oct 2	oct 9	oct 16	oct 23	oct 30	nov 6	nov 13
3D print of the cooling distributor (right)												
Drilling holes on the RICH for the N2 distributors												
Fix of the main leaks on the RICH												
Full EPanel assembly												
Test of the spherical mirrors (surface, reflectivity)												
Drilling wire holes on the top frontal panel												
Assembly test of the 3 cm aerogel layers												
Assembly test of the patch panels												
Assembly of the cosmics box on the EPanel												
Stiffening tool load test												
Full EPanel test with cosmics												
Cooling system on the full EPanel												
Assembly test of the brackets of the strong-back												
Cut of the frontal pillar from the trolley												
Assembly test of the mounts on the trolley												
Cleanup of the clean room												
Installation of the spherical mirrors												
Test of the nitrogen system on the cosmics box												
Setup of the N2 system for the RICH transportation												
Installation of the lateral mirrors												
Services in Hall B												

#### October:

**RICH Component Assembling** 

Photon Detector Commissioning

Steady Cosmic Run

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# Assembling Schedule

	WEEK											
activity	aug 28	sep 4	sep 11	sep 18	sep 25	oct 2	oct 9	oct 16	oct 23	oct 30	nov 6	nov 13
Installation of the exit panel												
Installation of the stiffening tool												
RICH in vertical position												
Alignment of the spherical mirrors												
Alignment of the lateral mirrors												
Installation of the bottom mirror												
Survey of the RICH												
Installation of the EPanel												
Installation of the patch panels on the RICH												
Installation of the frontal panels												
Test of the N2 system on the RICH												
Light-tightness test												
De-installation of the frontal panels												
Final assembly of the 3 cm aerogel layer												
Final assembly of the 2 cm aerogel layer												
Installation of the frontal panels with the aerogel												
Transportation of the RICH in Hall B												
Installation in CLAS12												

November: Final Assembling Validation Installation

Week of 30 October:

RICH Services in the Hall

Week of 13<sup>th</sup> November: RICH in the Hall