Electronics

Frontend Prototype Status

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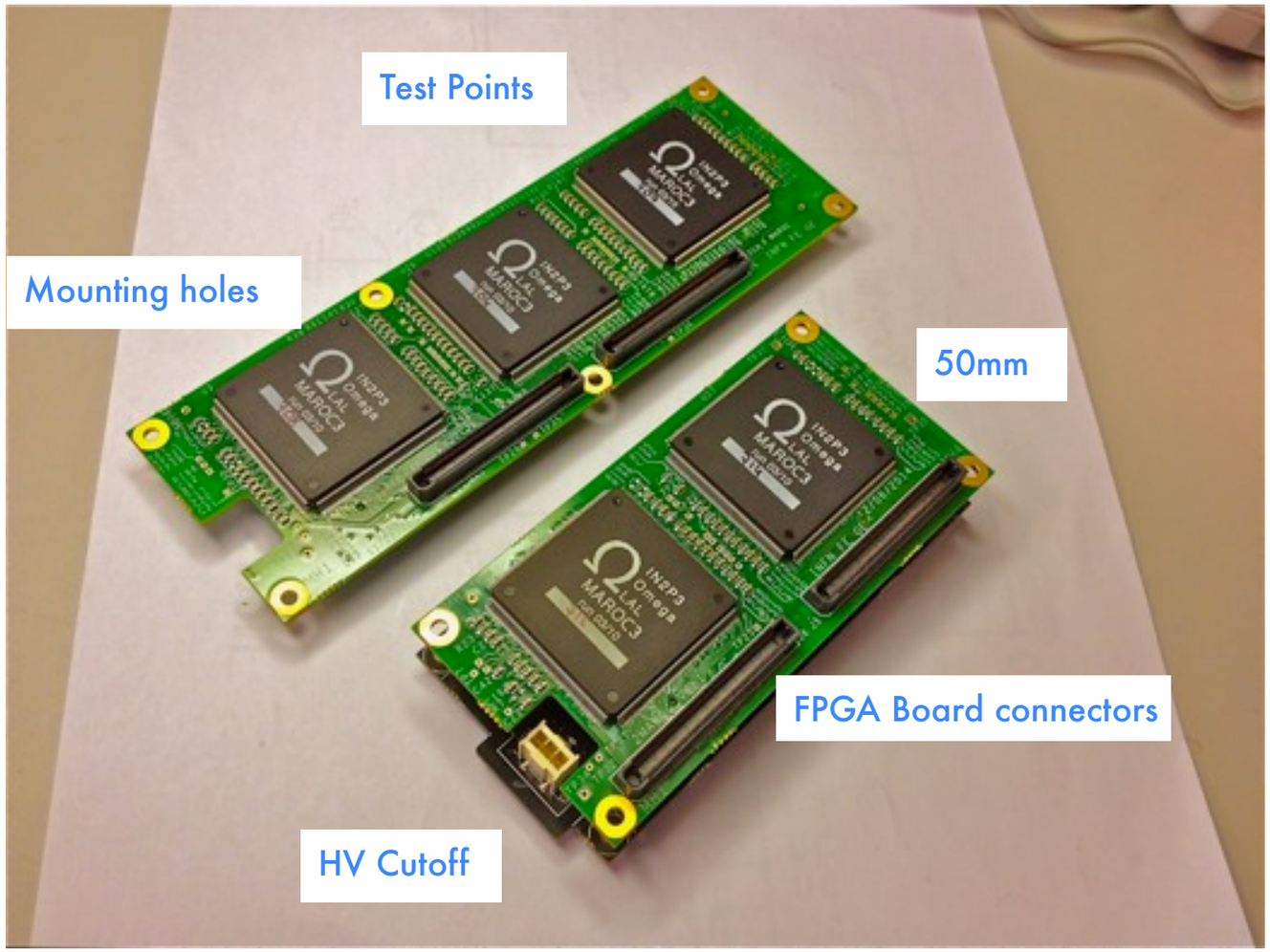
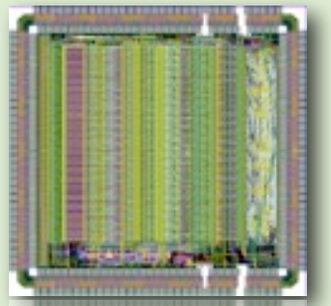
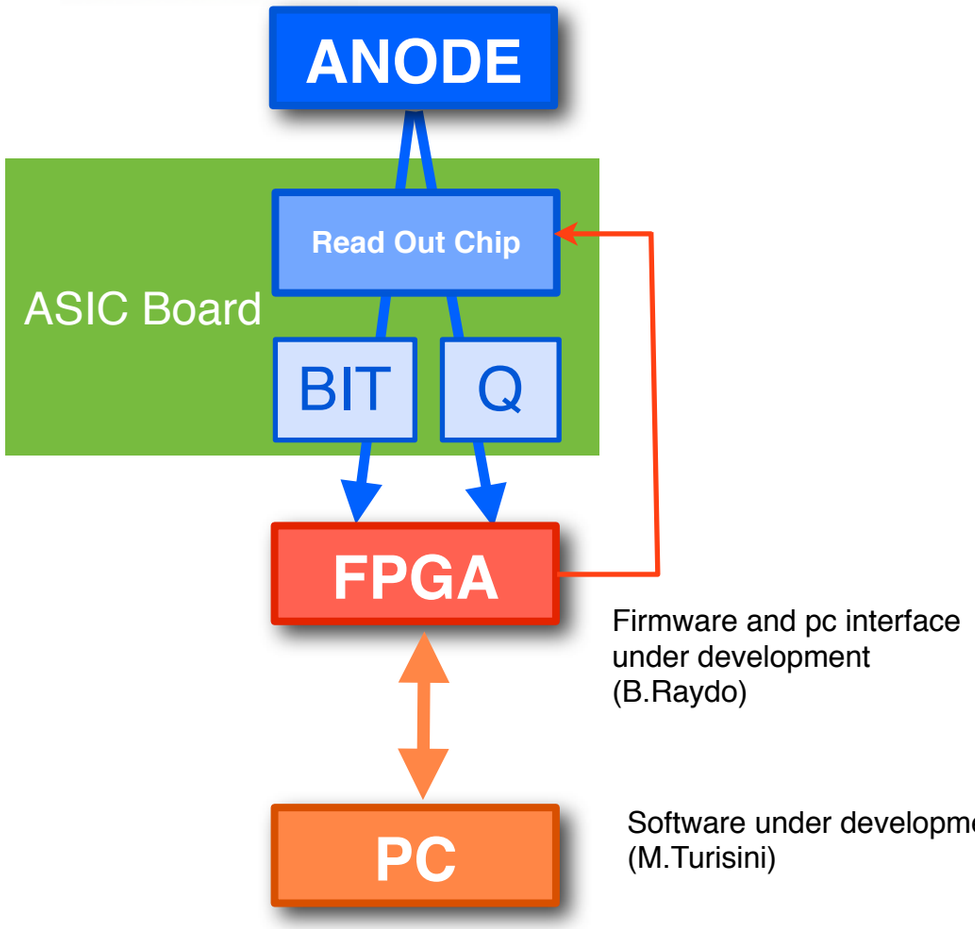
RICH Collaboration Meeting, 2014 November 12th

Intro





Multi **A**node **R**ead **O**ut **C**hip
version 3
64 Channels
by Omega Group
Application Specific
Integrated Circuit (ASIC)



Single Channel Block Schematics

- ASIC Boards available from October 15th
- 2 versions: 192 or 128 mapmt pixels discriminated outputs
- Need just one firmware version (*shift register test*)
- C/C++ software for configuration and measurements
- ROOT framework for analysis
- Open source library

Status and Perspective

4 Systems (10 ASIC +4 FPGA) PRODUCED
Basic electrical tests: ALL PASSED
Naked boards : PRODUCED for thermal and mechanical tests

Individual ASIC Configuration: READY
Characterization: STARTED
Readout development: STARTED
Software library: PRELIMINARY DESIGN

- Fully featured firmware available shortly
- Data acquisition and analysis software ready for the beginning of next year

Open question (asic boards):

- charge measurements, onChip or onBoard?
- calibration with onBoard charge injector, how many charge levels?

Fitting into CLAS12

Wiring:

- 3 type of cables (HV,LV,OPTICAL)
- 138 cables for type 4 meters long each (Simplified model)
- Solutions under development…

	CABLE	Diameter [mm]	Weight [gr/mt]
HV	RG58	5	35
LV	ALPHAWIRE 58124	4	43
OPTICAL	(custom*)	2	28

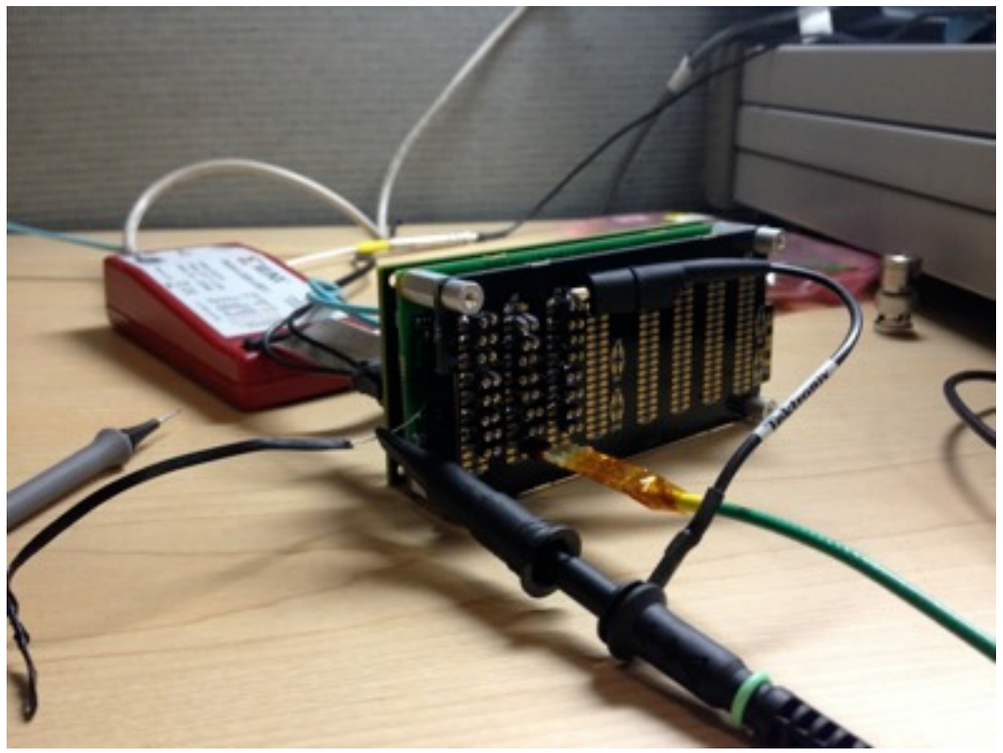
Preliminary

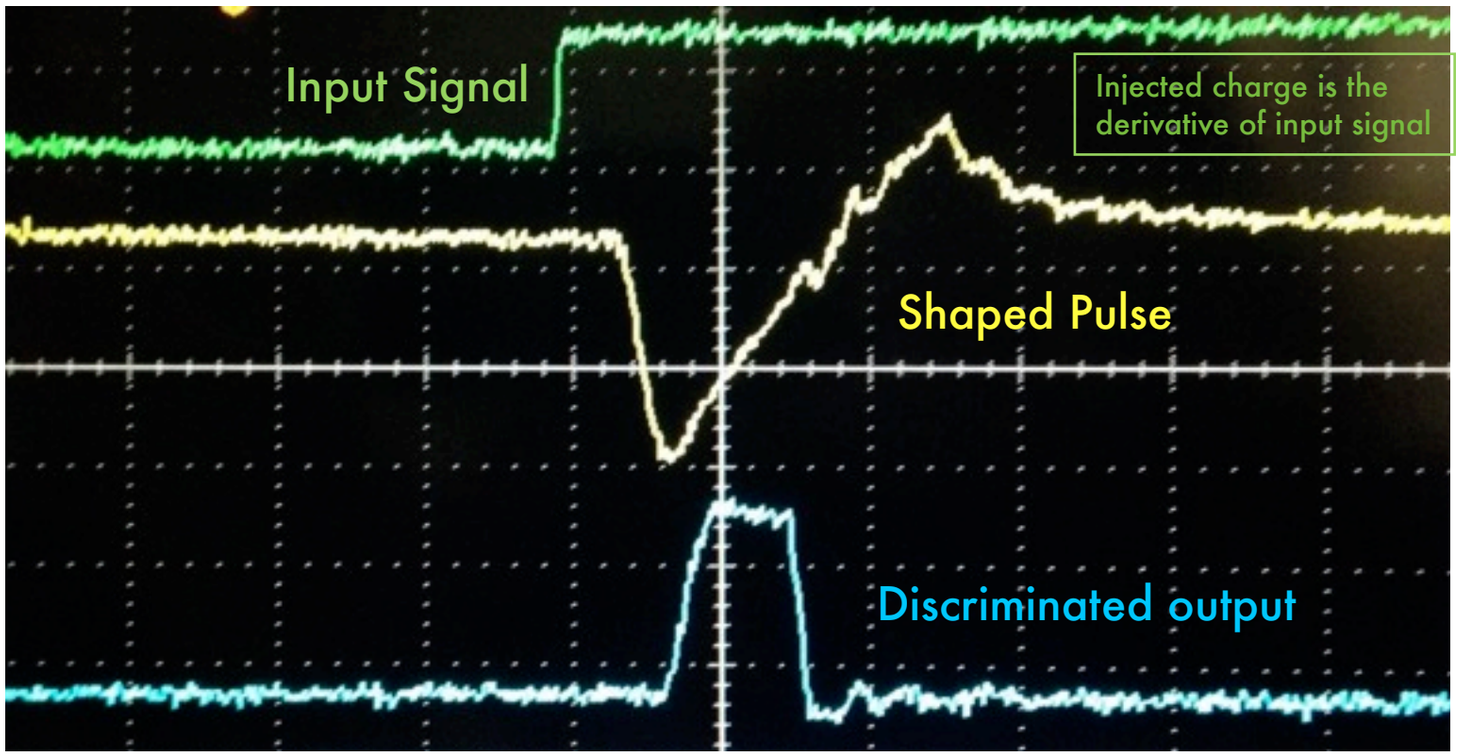
*multicore cable will be used

Heat production:

- single ASIC absorption = 62mA
- total ASIC boards power consumption = 100 W
- -20% turning off unused subcircuitry: to be tested
- FPGA board power consumption 0,7W
- could increase up to 3W depending on the fw
- Measurements scheduled on early 2015

Test setup: charge injectors

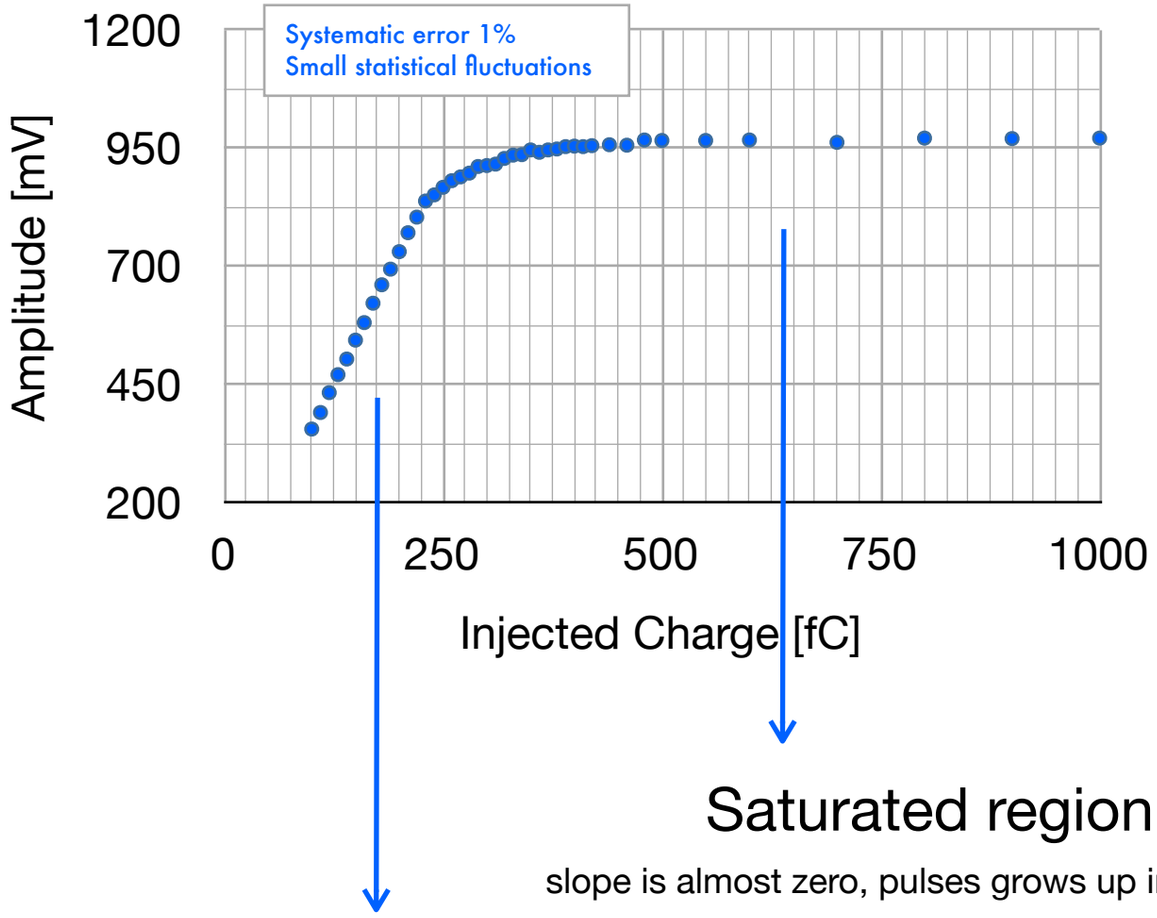




- TCP/IP fast ethernet protocol to communicate with front end (ping FPGA board 30 μs)
- FPGA flashing easy to use
- ASIC configuration debugged
- External charge injector setup ready (left picture) SPE level
- Onboard charge injection tested with scalers array
- Probing signals allow for test and characterize ASIC response (right picture and next slides)
- In the next month we will go ahead in parallel (JLab and INFN)
- MAPMT readout after completion of charge response studies

Example1: Shaping Characterization

Fast Shaper Gain

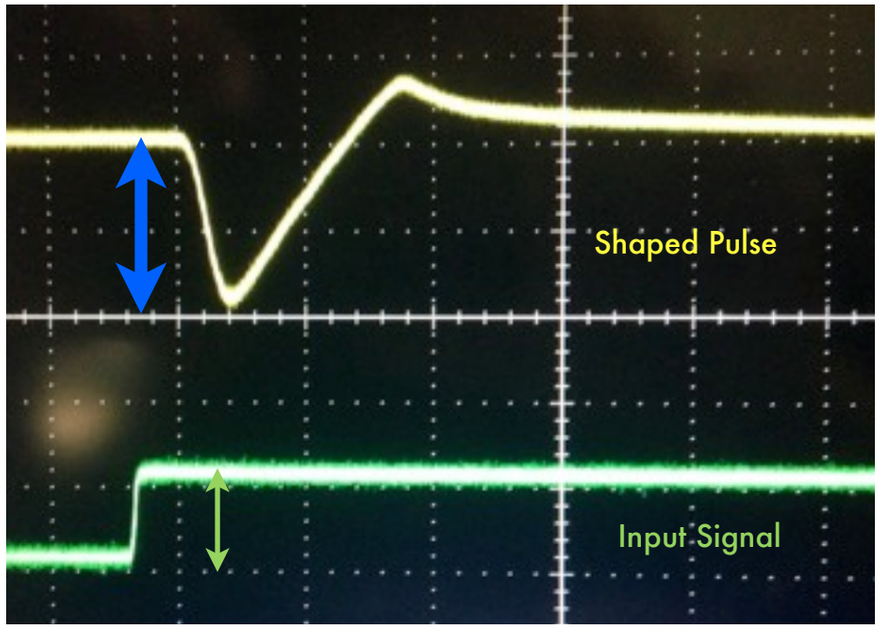


Linear region

3.75 mV/fC

Saturated region

slope is almost zero, pulses grows up in duration



Injected charge is the derivative of input signal

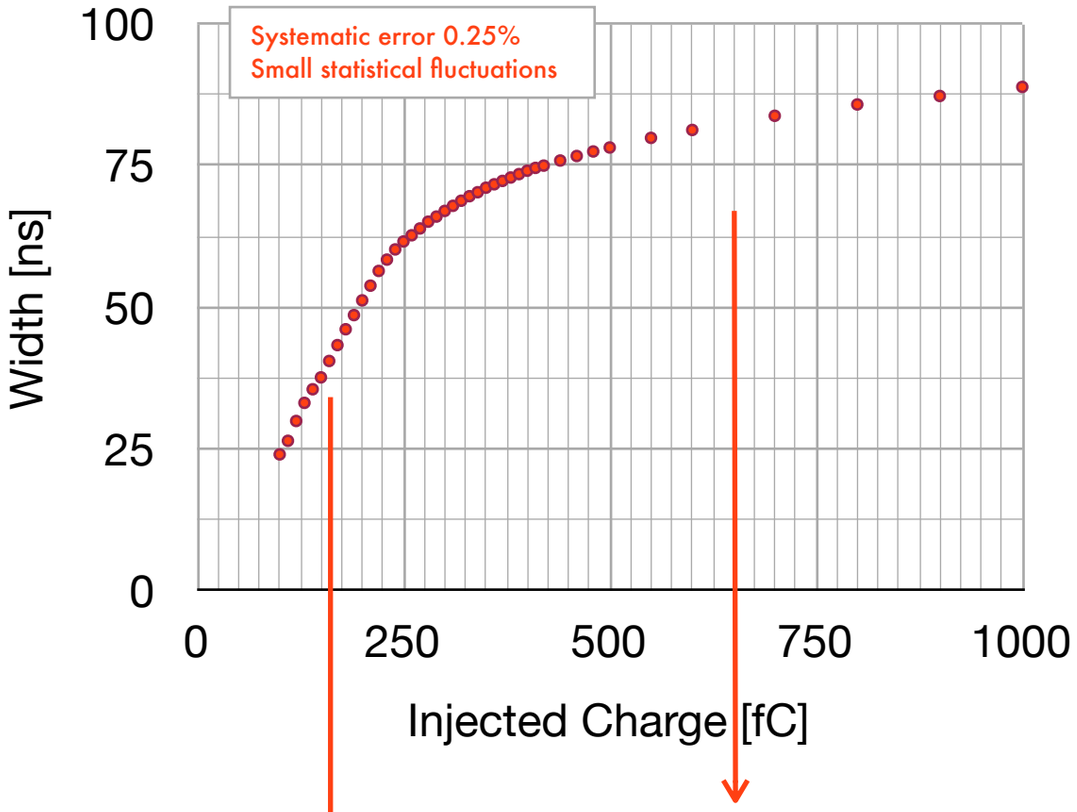
PLAN: characterize all the the shaping configuration offered by MAROC. Linearity region can be extended or reduced by changing the feedback network of the amplifiers.

Higher gain than Slow Shaper:

better signal to noise separation
improved spe resolution
better light yield than test beams at CERN!

Example2: Binary Output Characterization

Time over Threshold - FWHM

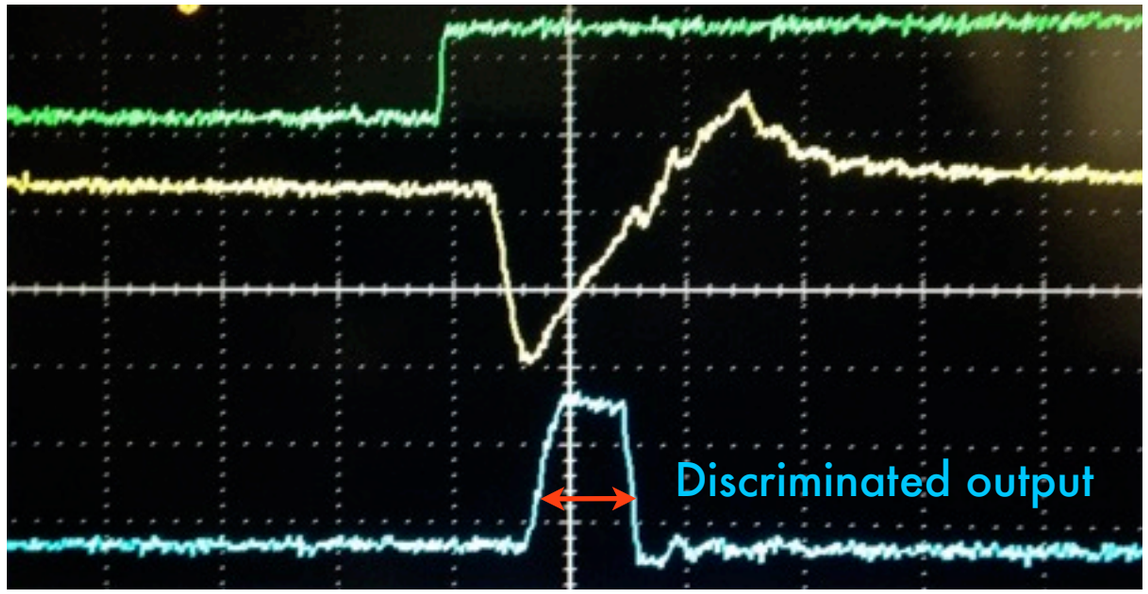


Linear region

270 fs/fC

Weak dependance region

(~logarithmic)



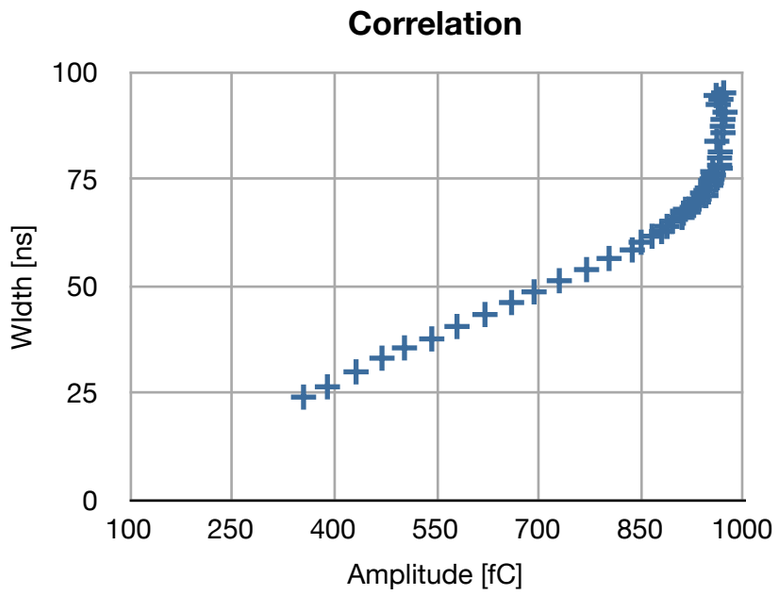
Full Width Half Maximum (FWHM)

First Time over Threshold ever for us!

Nice behaviour and very precise response

jitter upper limit 200ps (satisfy RICH design requirements)

Allow time over threshold charge measurements with a good resolution



Amplitude of the shaped pulse
Width of the discriminated output

Conclusion

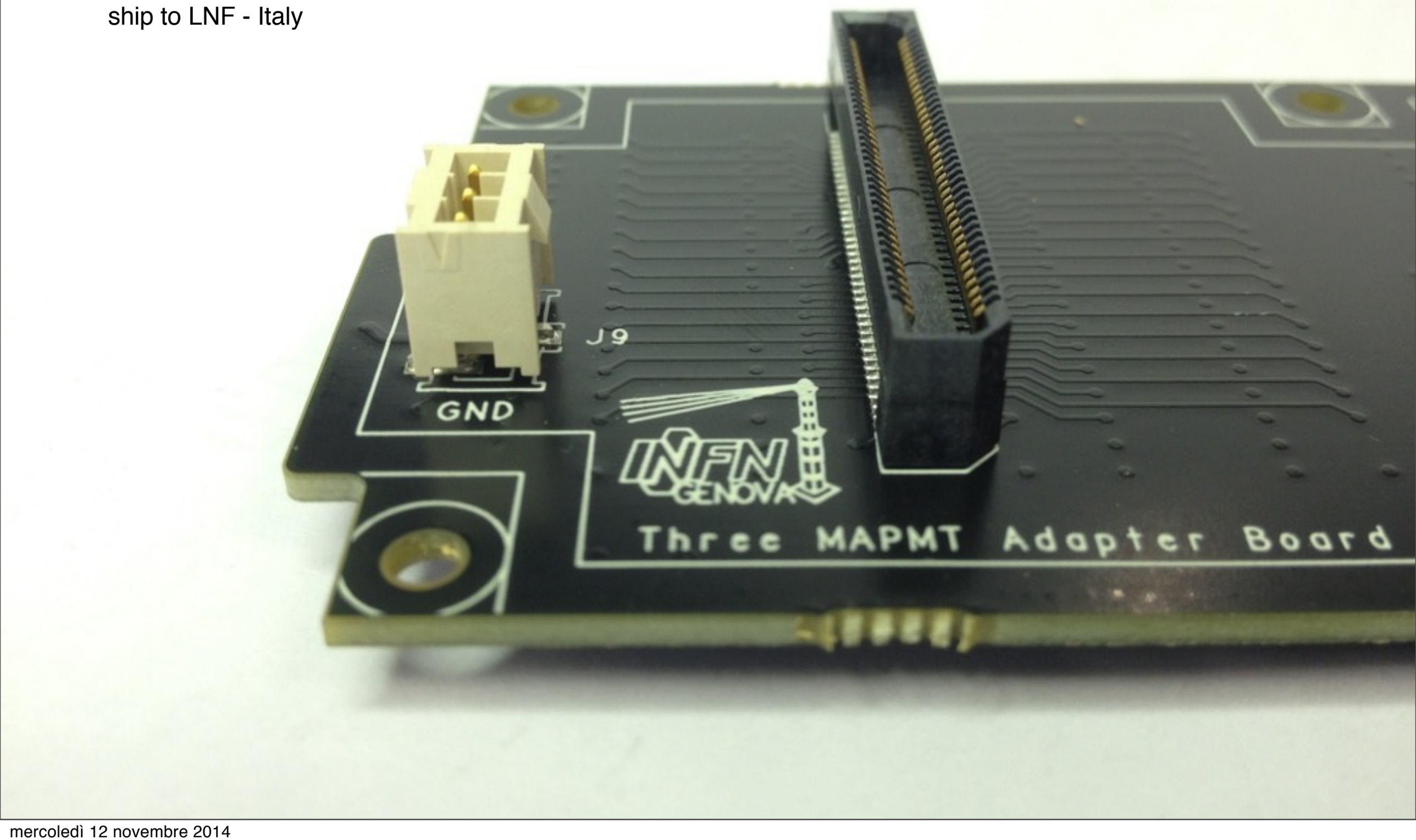
1. Frontend boards prototype are clean and well made
2. We are on schedule or even in advance
3. First test showed no issues in communication and good discrimination performance
4. Characterization and development will proceed in parallel between JLab and INFN
5. We can decide the definitive design of the boards with calm after having performed a complete set of studies.

Backup slides

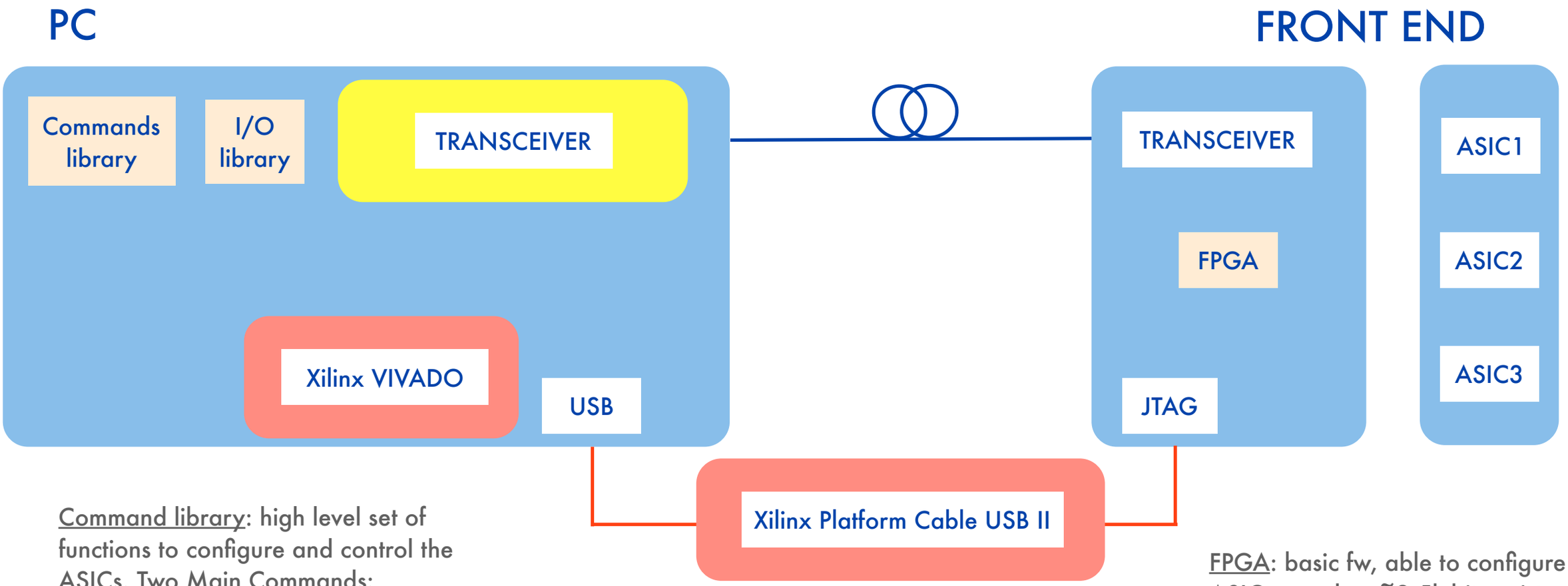
Adapter Boards

Naked + Adapter

For mechanical tests
ship to LNF - Italy



Setup for devel/debug



Command library: high level set of functions to configure and control the ASICs. Two Main Commands:
1.Configure
2.ReadOutConfiguration*

I/O library: a low level software module for communicating with the FPGA using UDP Ethernet protocol on Optical Link.

FPGA: basic fw, able to configure ASICs, needs a ~2.5k bit register (one maroc slow control 829 bit) and a routine for shifting it inside the ASICs.

Thanks to Benjamin Raydo and Luca Barion for their positive support

*Would be nice to have the possibility to readout actual slow control directly from the MAROC (when not running!)
To check the correctness of the configuration.

Basic Validation Test

Tested 4 ASIC BOARD (i.e.10 MAROC)

BOARD_ID	*N_ASIC*	*Current*	*VDDD*	*VDDA*	*VH_HSTL*	*VREF_33*	*V_BG*		
			C88	C87	C114	C58	TP8	TP18	TP12
		[mA]	[Volt]						
#1	2	140	3,318	3,497	1,817	3,003	2,448	2,461	no
#2	2	140	3,309	3,500	1,818	3,003	2,436	2,426	no
#3	3	207	3,284	3,492	1,811	3,000	2,410	2,426	2,403
#4	3	187	3,279	3,493	1,809	3,000	2,418	2,379	2,446

V_BG = ASIC's internal voltage band gap. Used to determine chips integrity.

The expected value of 2,4 Volt has been observed for all the 10 chip on board.

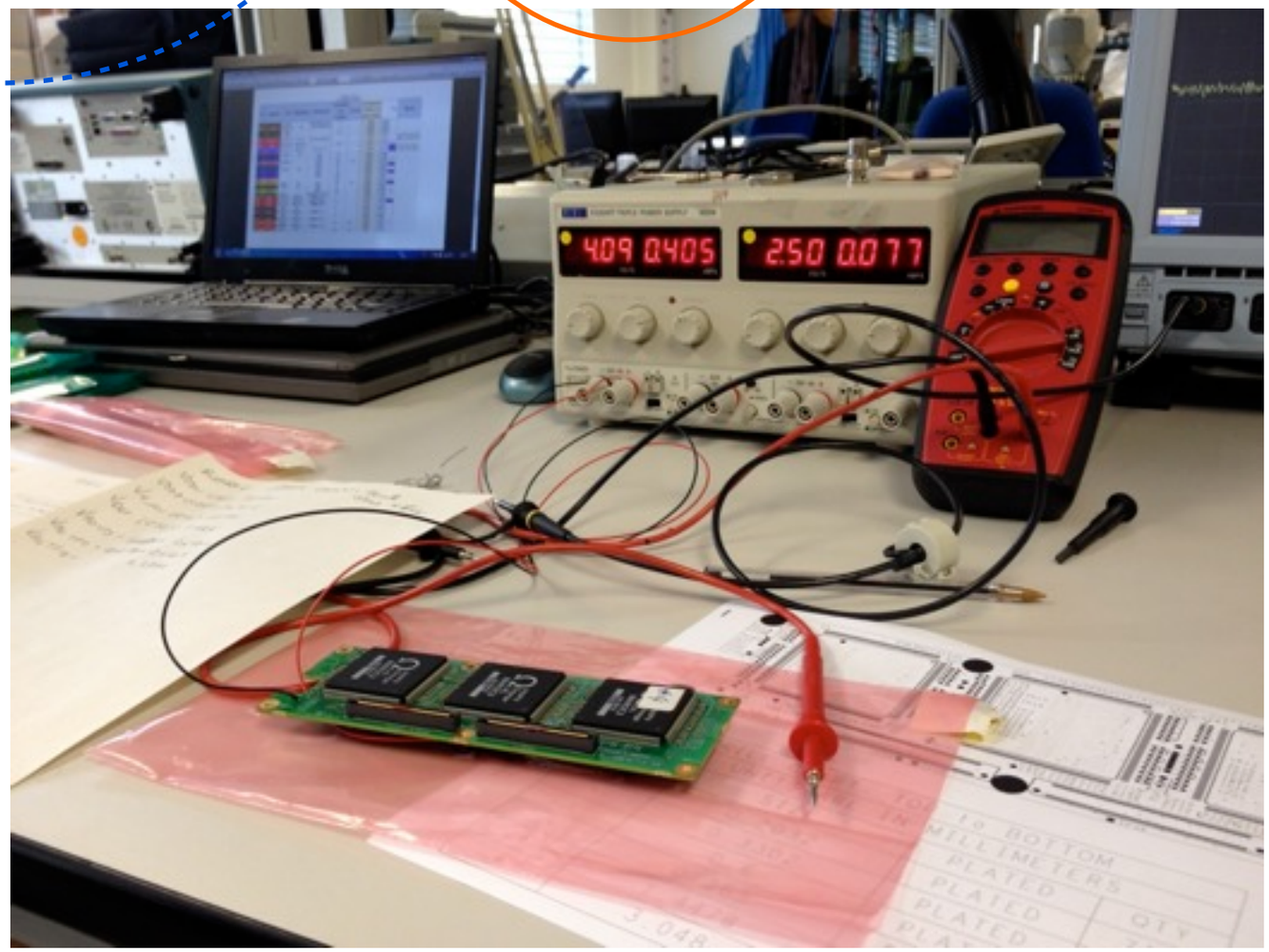
Onboard regulated voltages have been measured.
All values are compatible with the design pecifications

ASIC Board current absorpitons are consistent with MAROC datasheet

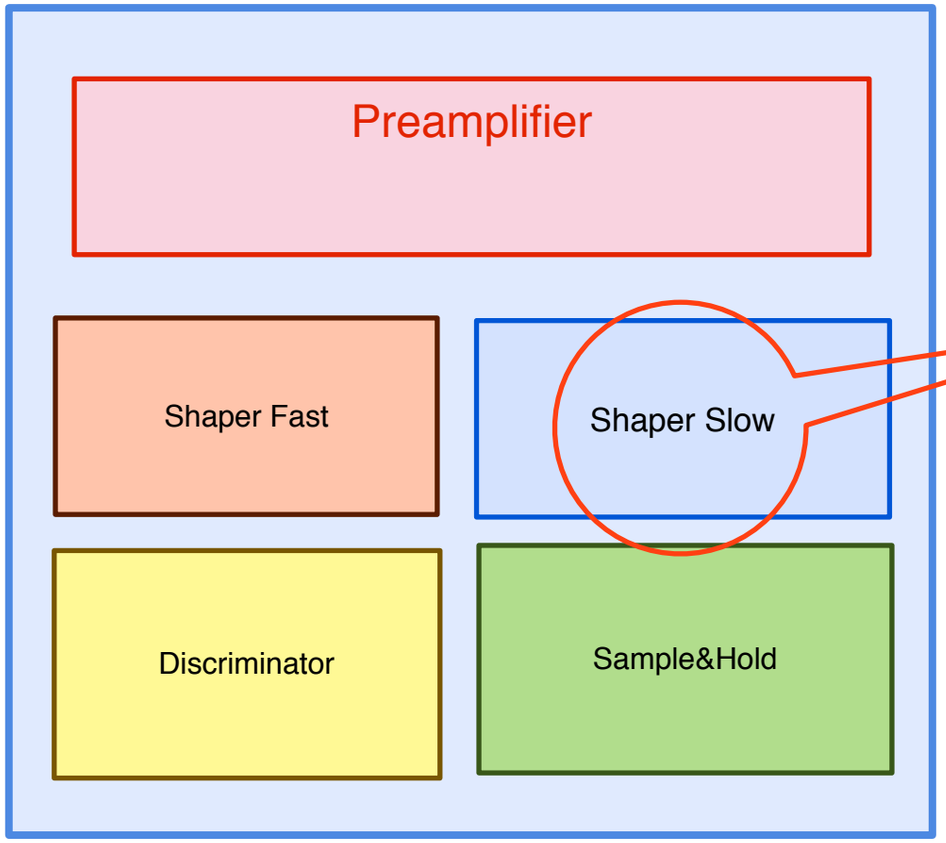
1,1 mA / channel

3,8 mWatt / channel

100 Watt / sector



MAROC details



MAROC single channel