RICH Frontend Validation Test

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ASIC Board

New boards
received this week
in Ferrara

4 ASIC boards in
(3+3+2+2)

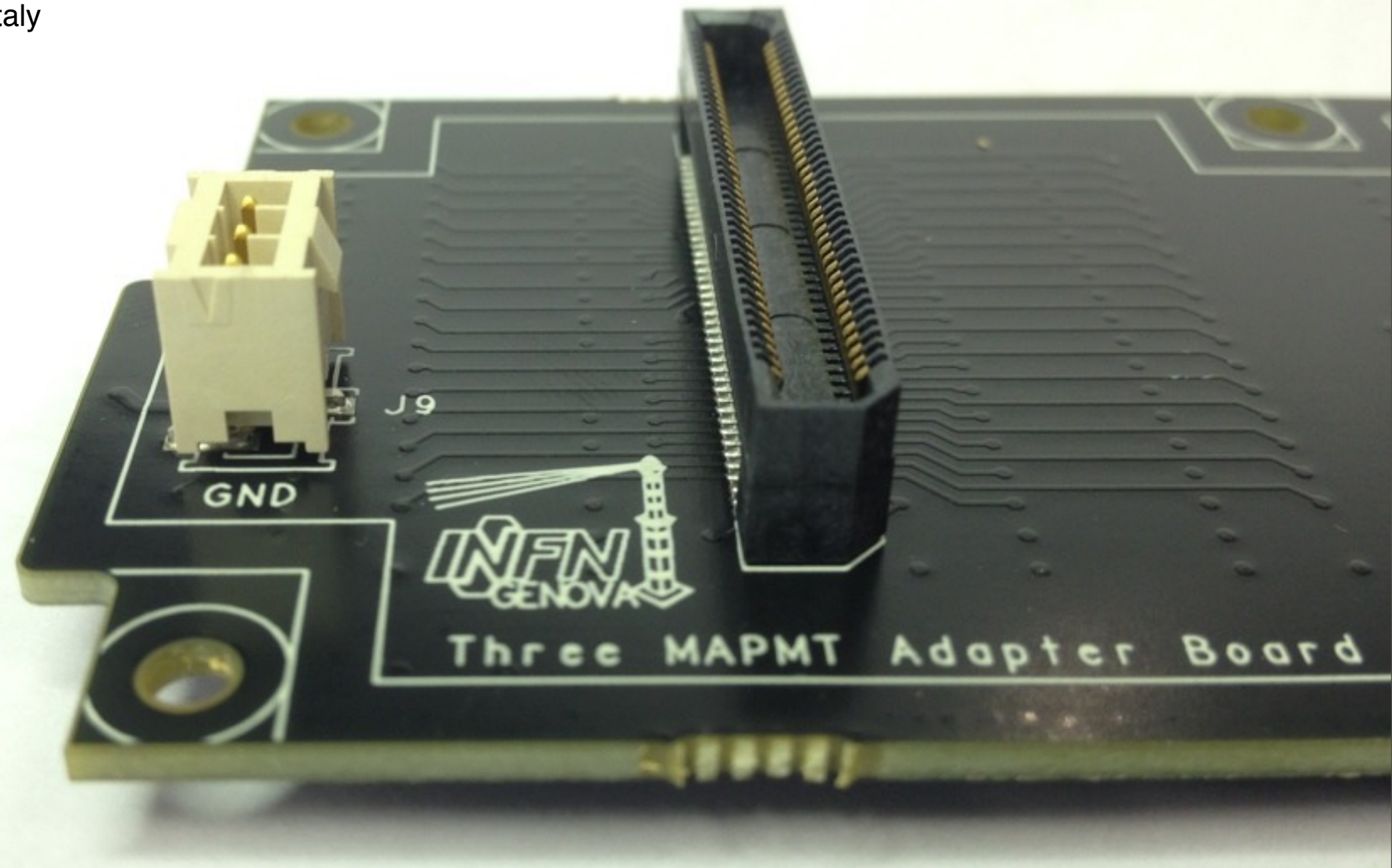
All passed
validation test
(see slide 3)

For development and debug
half of them to JLab
the other half stay in Ferrara

Prototype Boards

Naked + Adapter

For mechanical tests
ship to LNF - Italy



Validation Test

Tested 4 ASIC BOARD (i.e.10 MAROC)

BOARD_ID	*N_ASIC*	*Current*	*VDDD*	*VDDA*	*VH_HSTL*	*VREF_33*	*V_BG*		
			C88	C87	C114	C58	TP8	TP18	TP12
		[mA]	[Volt]						
#1	2	140	3,318	3,497	1,817	3,003	2,448	2,461	no
#2	2	140	3,309	3,500	1,818	3,003	2,436	2,426	no
#3	3	207	3,284	3,492	1,811	3,000	2,410	2,426	2,403
#4	3	187	3,279	3,493	1,809	3,000	2,418	2,379	2,446

V_BG = ASIC's internal voltage band gap. Used to determine chips integrity.

The expected value of 2,4 Volt has been observed for all the 10 chip on board.

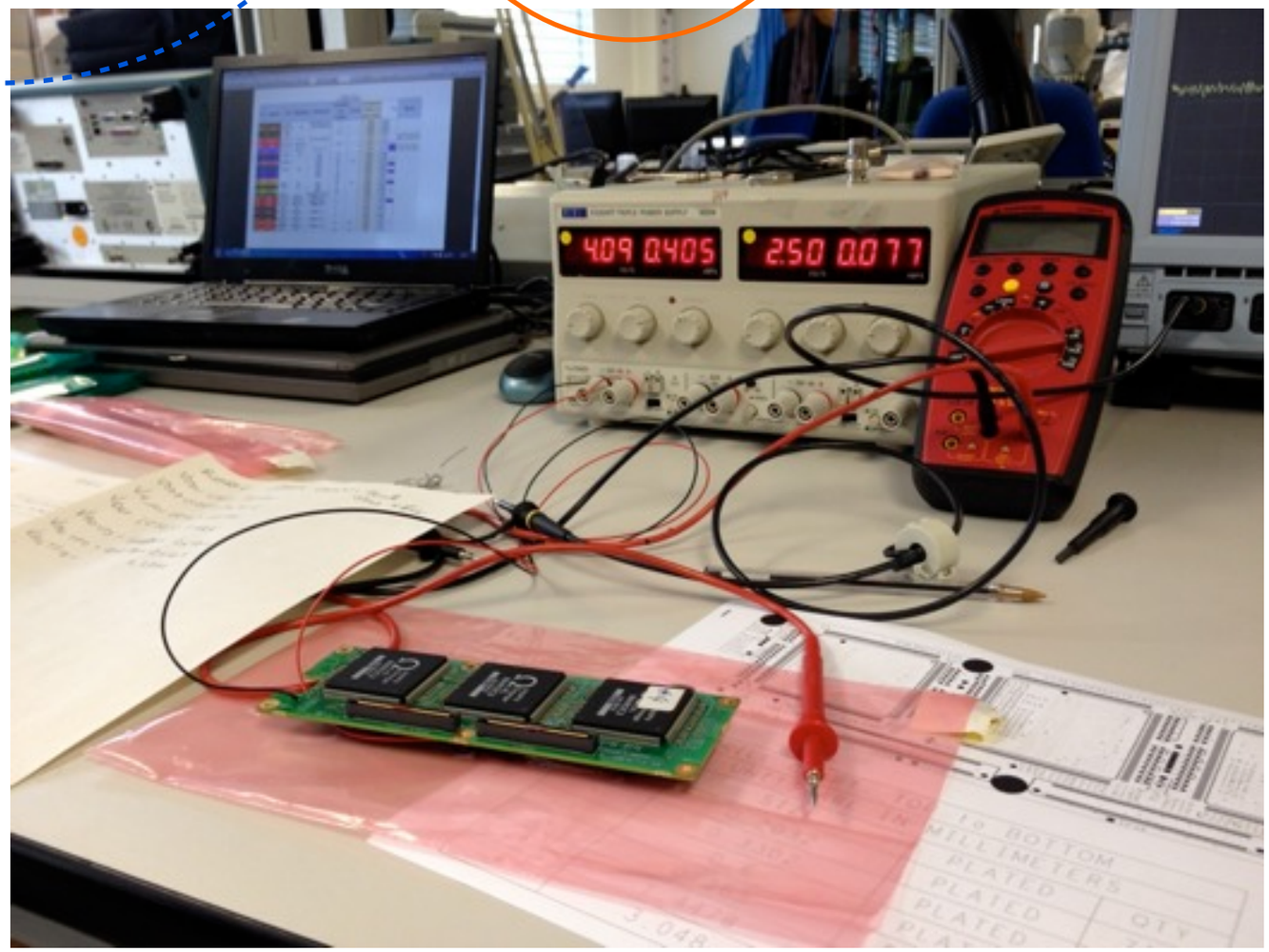
Onboard regulated voltages have been measured.
All values are compatible with the design pecifications

ASIC Board current absorpitons are consistent with MAROC datasheet

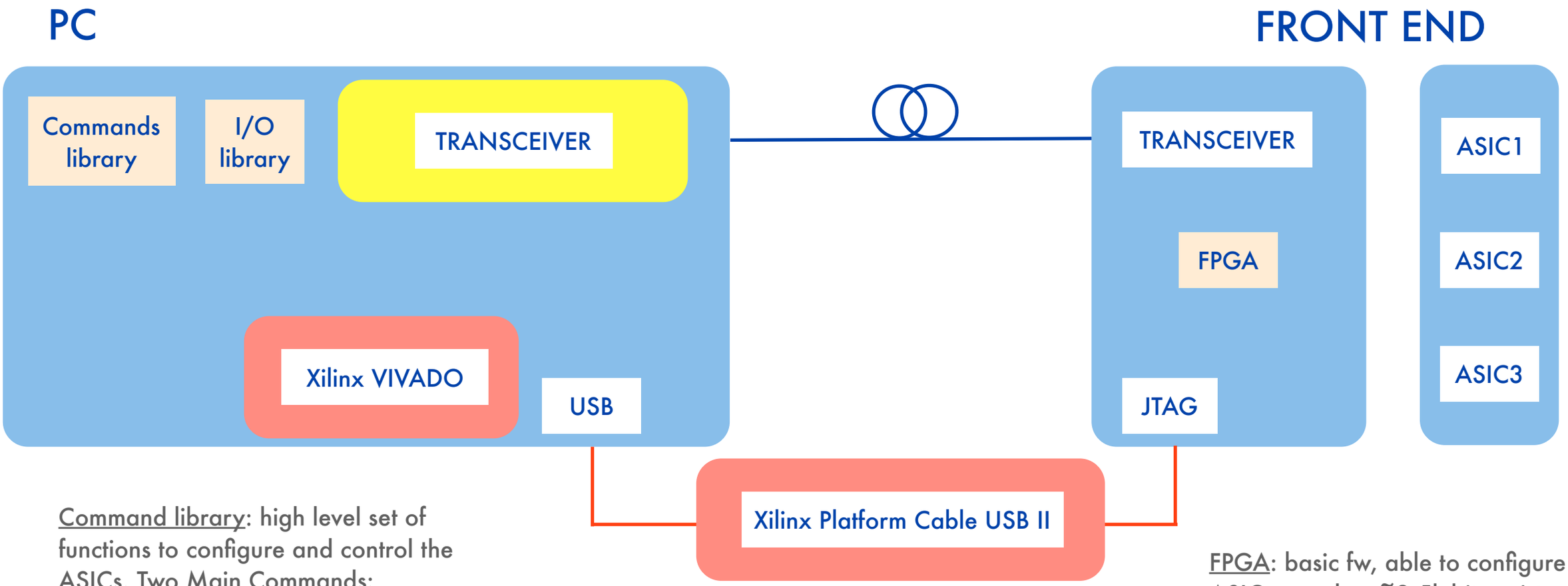
1,1 mA / channel

3,8 mWatt / channel

100 Watt / sector



Setup for devel/debug



Command library: high level set of functions to configure and control the ASICs. Two Main Commands:
1.Configure
2.ReadOutConfiguration*

I/O library: a low level software module for communicating with the FPGA using UDP Ethernet protocol on Optical Link.

FPGA: basic fw, able to configure ASICs, needs a ~2.5k bit register (one maroc slow control 829 bit) and a routine for shifting it inside the ASICs.

Thanks to Benjamin Raydo and Luca Barion for their positive support

*Would be nice to have the possibility to readout actual slow control directly from the MAROC (when not running!)
To check the correctness of the configuration.

Summary

1. EES did a good job, new boards are clean and satisfy the elementary electrical specifications.

2. All the MAROC chips have passed the validation test. Boards are ready to be used.

3. Equipment will be shipped to Frascati and JLab next week. Two ASIC board will stay in Ferrara

4. Test Bench in Ferrara almost complete