ASIC Boards Status

1. Readout overview
2. Design status
3. Calibration studies

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Readout System

CLAS12 **RI**ng **CH**erenkov detector
single photon detection suface
1 m^2 with 25000 pixel (6mm x 6mm)

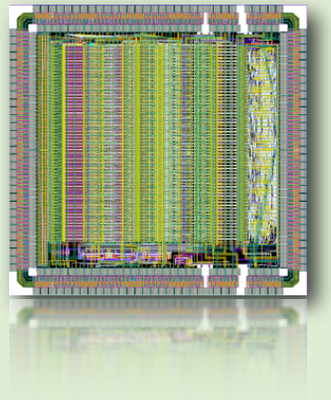
Event ***= {Hits , Timestamps, Positions}***

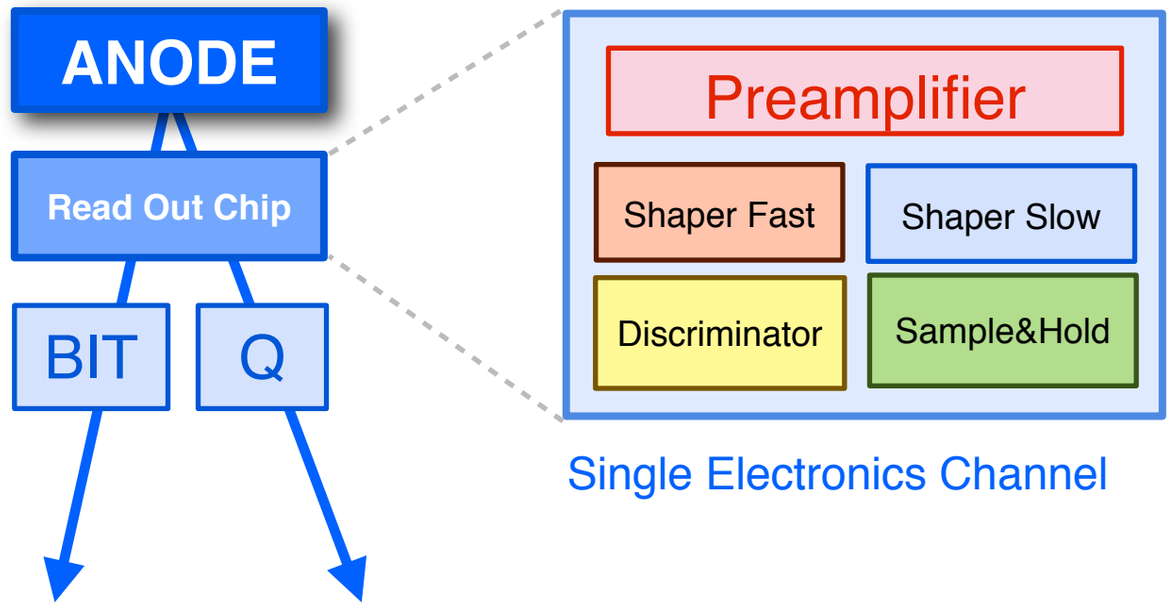
Signal Processing Clock Maps

Electronics Main Requirements

1 - Spe sensitivity
2 - Gain spread compensation1:4
3 - Trigger Rate 20kHz
4 - Latency 8 µs
5 - Time resolution ~1ns

Multi **A**node- **R**ead **O**ut **C**hip
version 3
64 Channel
3.5 mW/channel
by Omega Group
Application Specific
Integrated Circuit (ASIC)





Single Electronics Channel

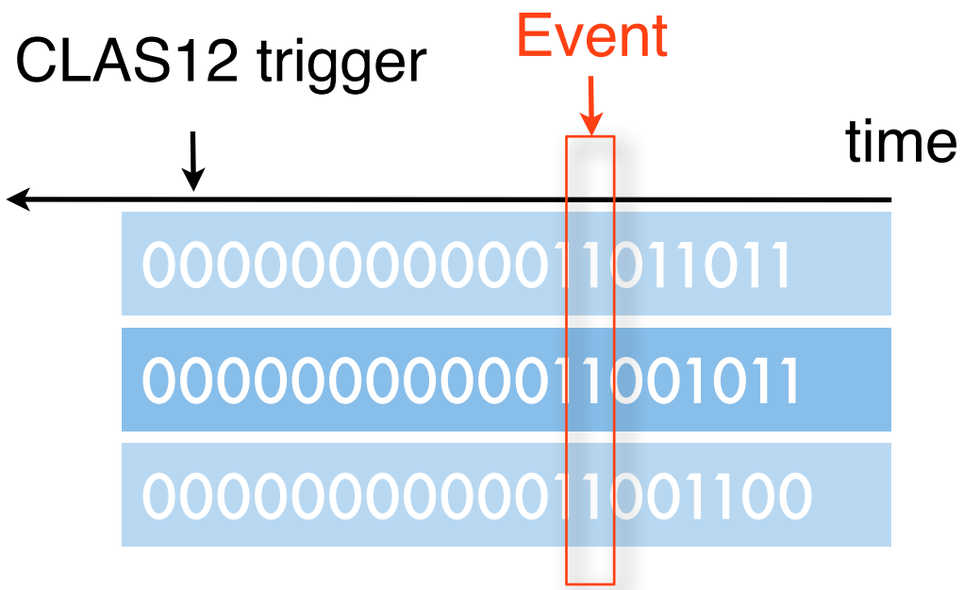
MAROC has two kind of output :
BINARY and ***CHARGE***

Binary vs Charge

BINARY:

- Prompt parallel line ***Fast***

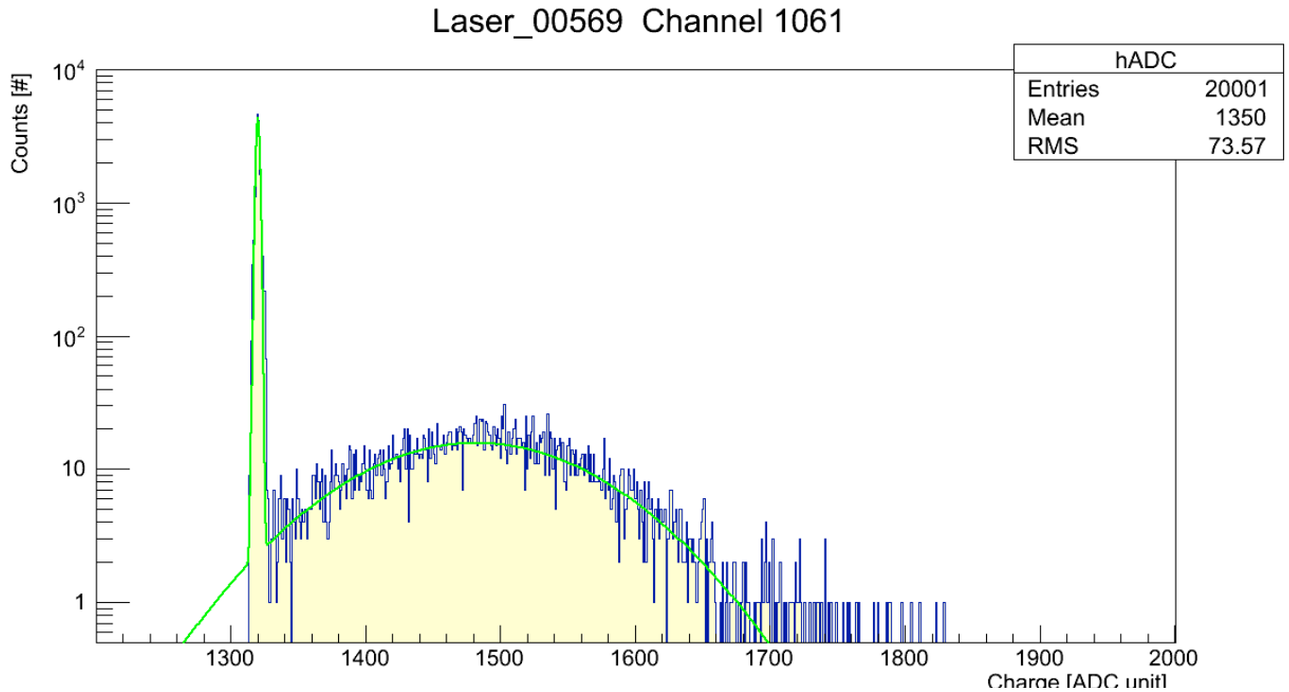
FIFO implemented at front end level (FPGA)



- In a ***FIFO*** with 8 µs max latency
- Cherenkov light directly imaged by **hardware discrimination**
- ***Compact*** description of events lead to a negligible dead time at 20kHz trigger rate

CHARGE:

- Serial line (Multiplexed) ***Slow***
- Contains many informations but inadequate readout time.
- Ring reconstructed by software
- Good for dedicated calibration runs

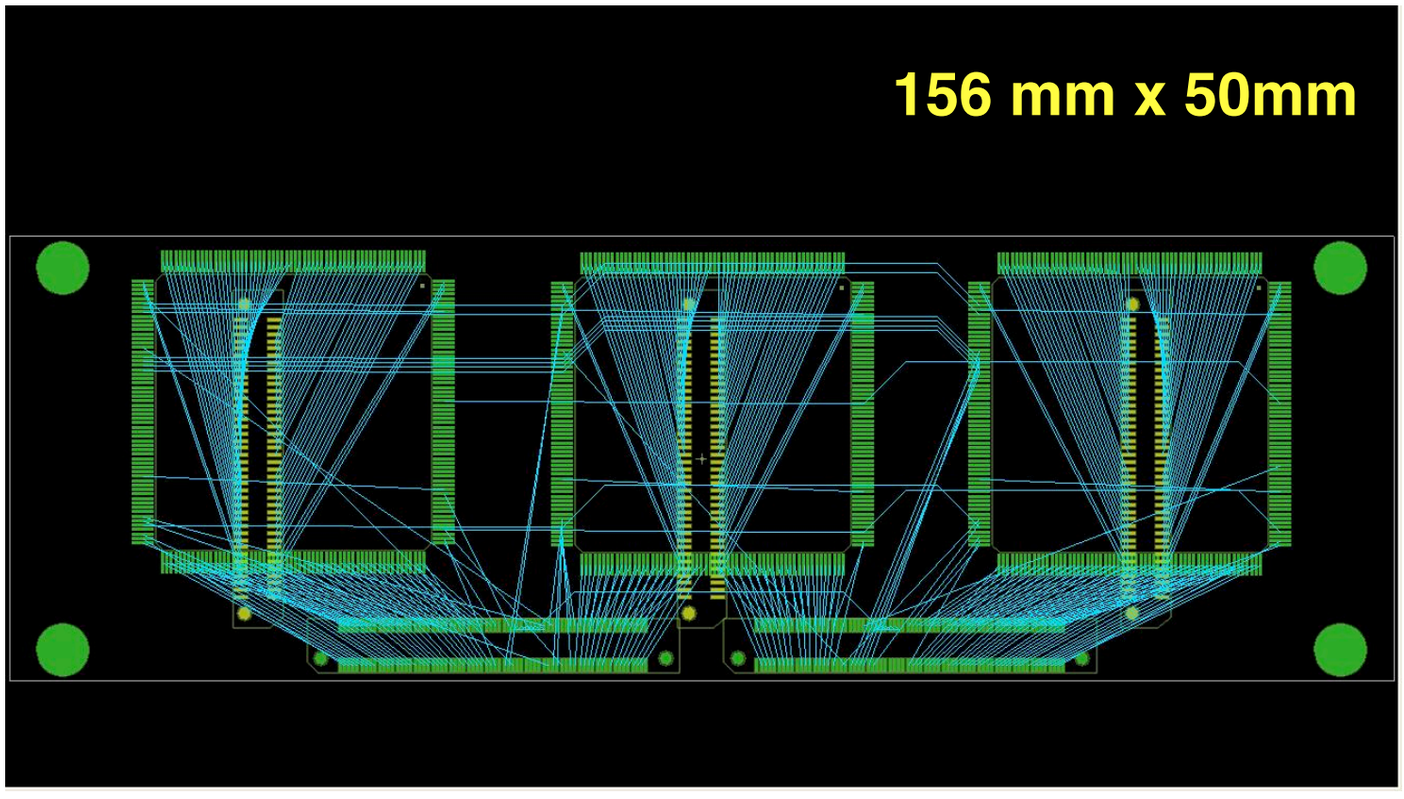


Charge spectrum with double gaussian fit

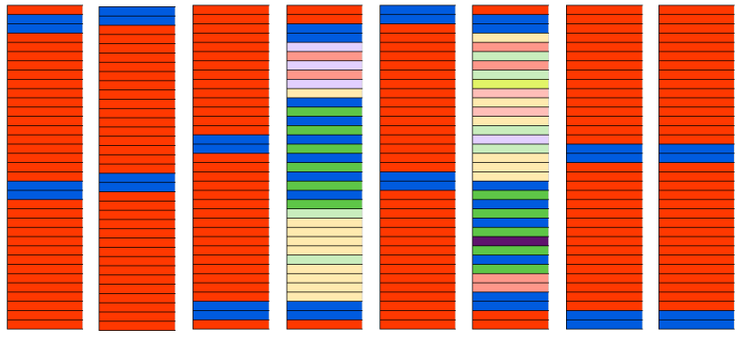
Comparison tests beam with RICH prototype scheduled in April 2014 at BTF Frascati, Italy.

Status of the front-end ASIC boad

I. Functional organization
II. Schematics
III. I/O assignment
IV. Placing and Routing



FPGA connections are the same in both version,
3 ASIC here, 2 ASIC next slide



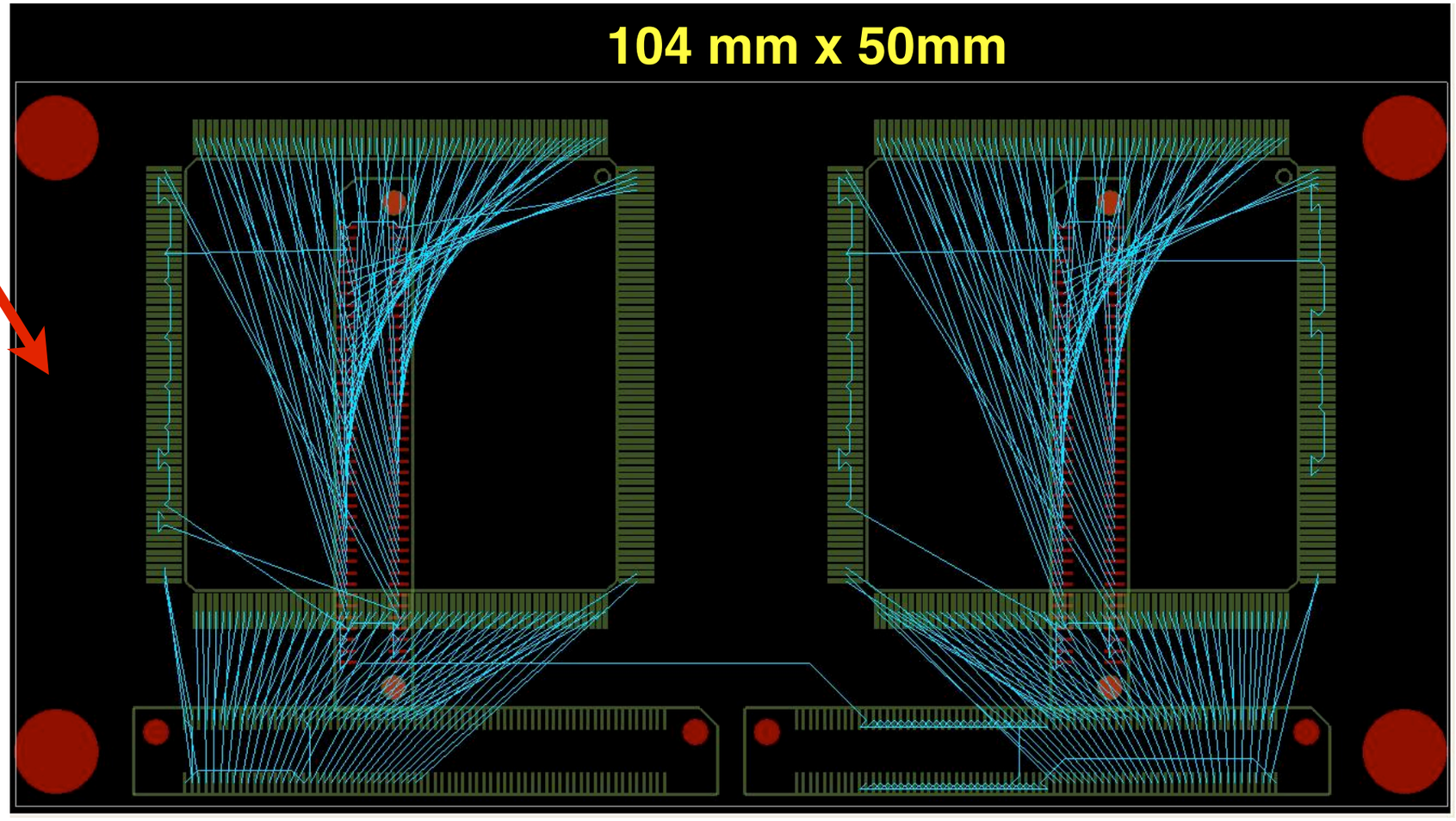
Connector organization
using color coding on the right
(280 pinsl)

I/O pins subgroups

BINARY OUT	Outputs
MASKED_OR	
Dynamic Register	Slow and Fast Controls
Static Register	
HOLD	
External ADC	Charge Measurement
Internal ADC	
Test Pulse	Parallel pin to inject a known charge in all the channel , 1,2 or 3 fixed chargesvalues
Power Supply	
Ground Reference	

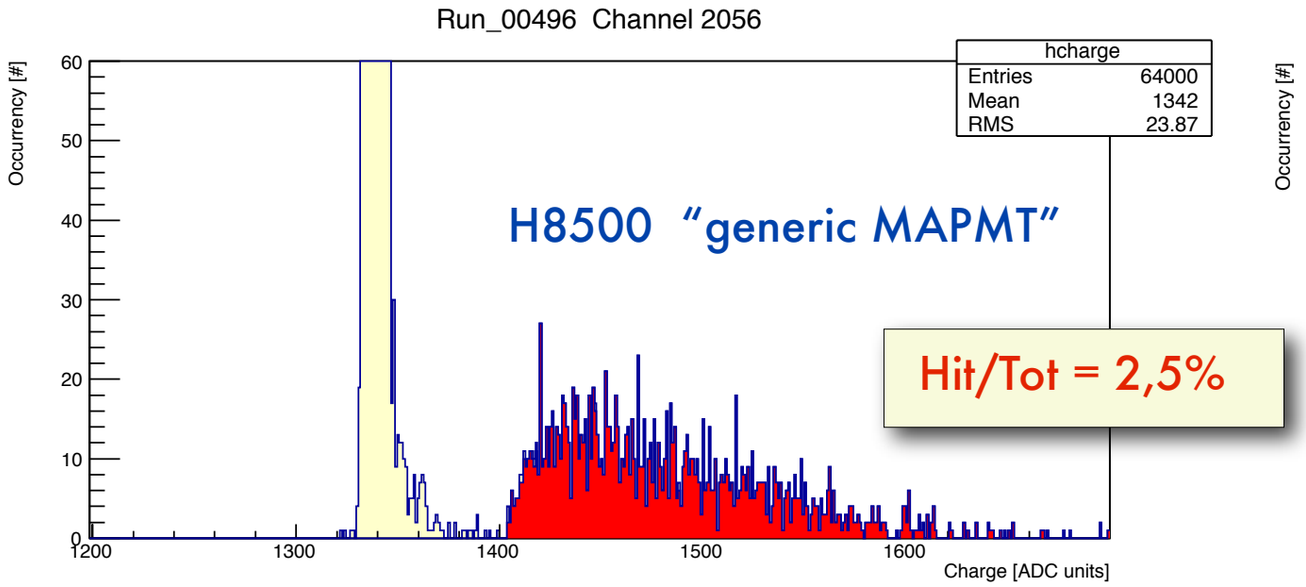
Status of the front-end ASIC boad

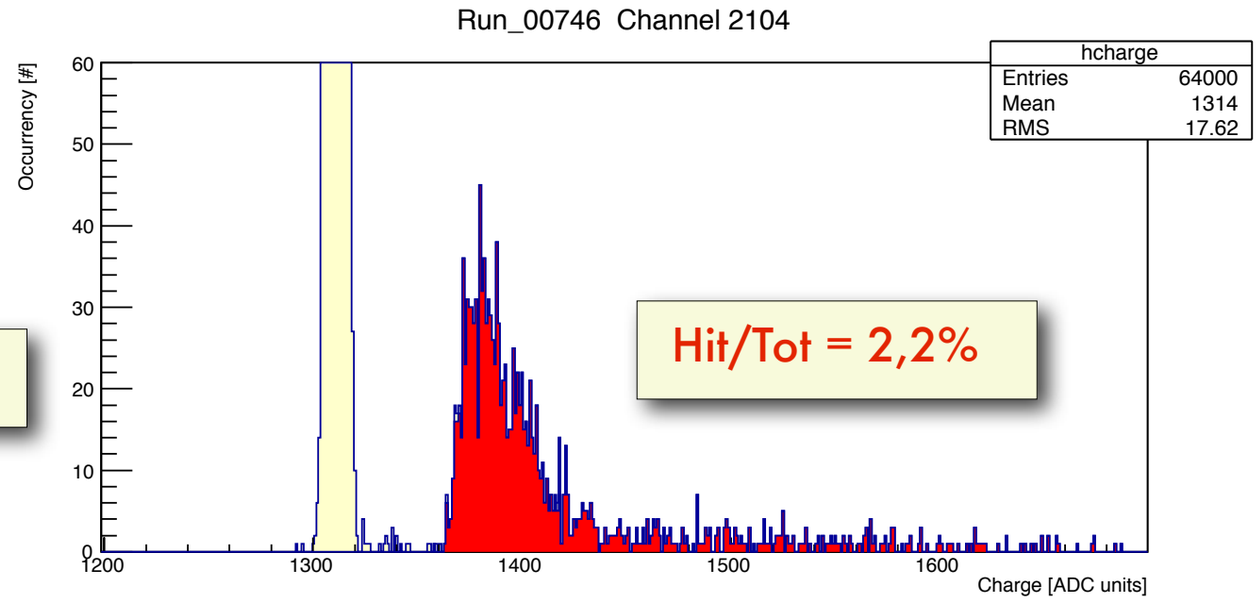
I. Gerber file, mechanical constraints into electric scheme (airflux & wiring cutoffs)
II. H8500 Adapter board
III. HV connector



Pins sequence is preserved when moving from 3 ASICto 2ASIC version

Self Trigger: H8500 and H12700 comparison





- High Signal / Noise on both devices
- Better single photon resolution on H12700 but very high dark rate on few channels

SELF TRIGGER

Simple OR on MAROC trigger bits triggers the charge measurements

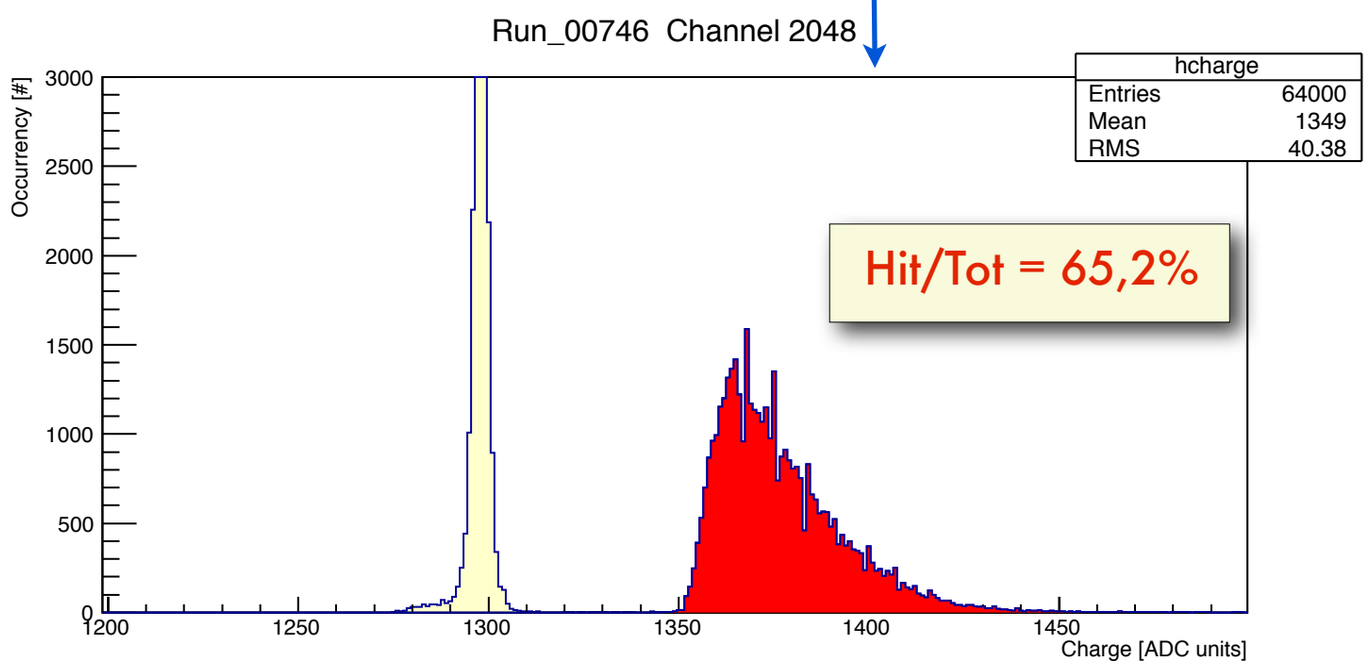
DARK Counts

- 10Hz/channel
- HIT/TOT = 1/64 (1,5%)

PLOTS

- 64kevts run
- same ADC range(x axis)
- no preamp tuning (GAIN=1)
- HV = 1000 Volt

H12700 "SPE dedicated"



{MAPMT-Front end} Workpoint

Goal

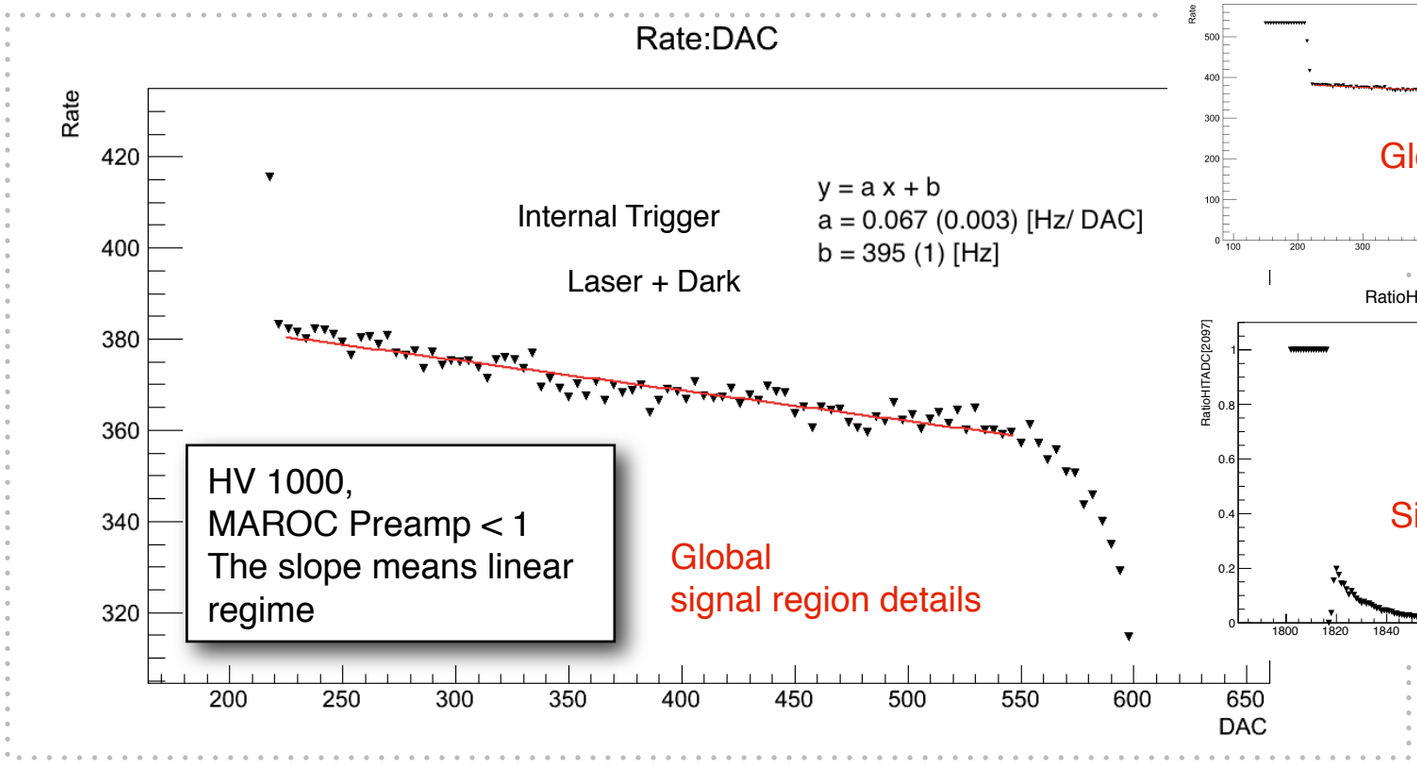
Define the best workpoint when maroc is used in binay readout.
HV as low as possible (1000V)

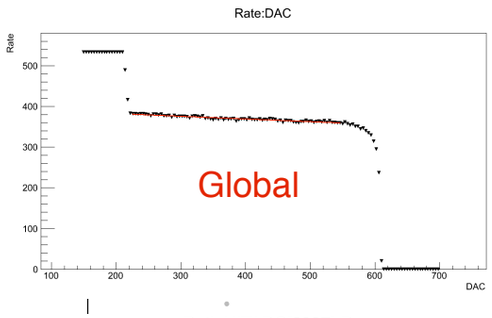
Under investigation

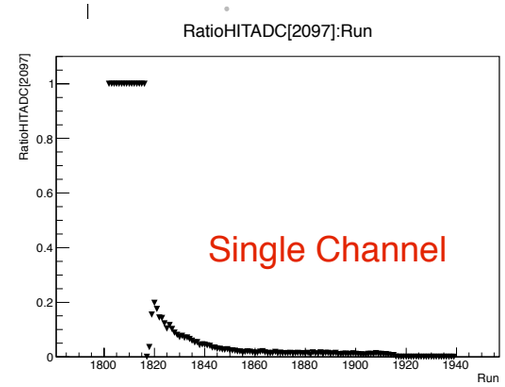
- Gain and dark frequency
- Gain ans ADC parameters

Strategy

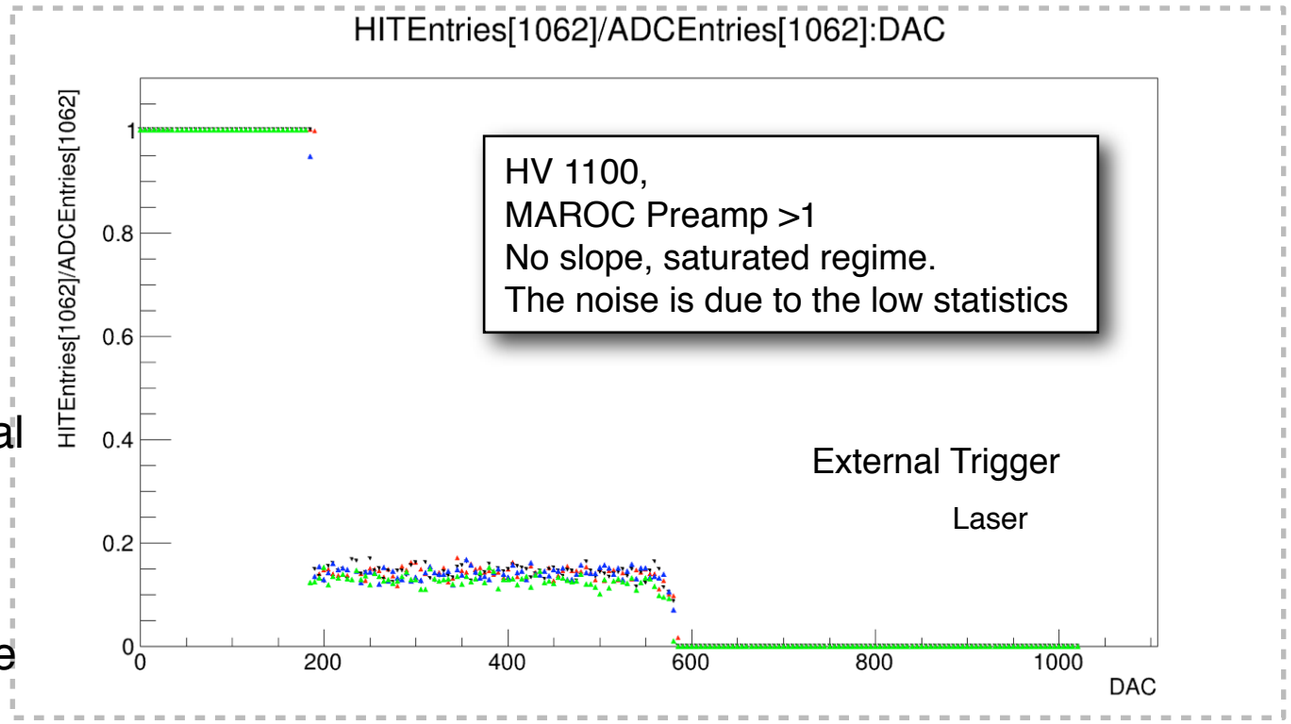
- use dark counts
- define intercalibration methods
- compare anlog and digital







- Multi Run Analysis
  X Axis
  Threshold scan
  [DAC unit]
- Y Axis,
  has Rate [Hz] or
  Efficiency [#hit/#total evts]
- Readout complete
  (all the channels are readout)



HV Recap

Higher the HV
higher the anodic charge

MAX H8500 hv = 1100 Volt
TYP H8500 hv = 1000 Volt

Test Bench =
1075,1040,1000
Test Beam =
1075,
(few runs 1040,1000)

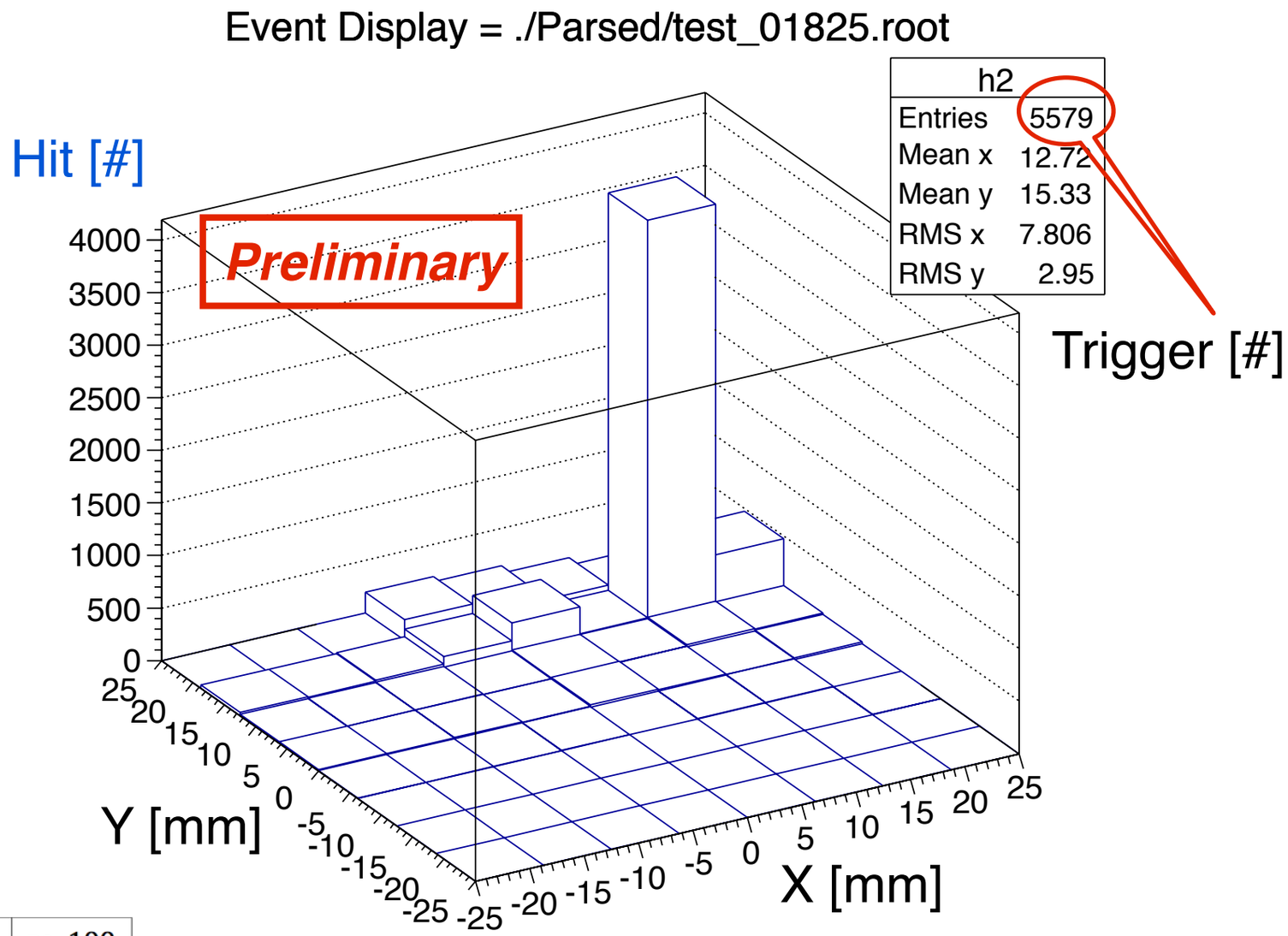
HighVoltage and PreAmp

SETUP:
- MAPMT Hamamatsu H8500
- Laser on one pixel
- Self Trigger Mode

Laser:
reference
adj freq
adj (mean)number of photon

Dark:
single photone HV

Tune up methodologies



MAPMT AA2112, HV = 1000 Volt,

Serial No: AA2112

Ratio of Anode Output= 1 : 1.5

P1: 79	P2: 81	P3: 76	P4: 72	P5: 75	P6: 84	P7: 94	P8: 100
P9: 70	P10: 69	P11: 71	P12: 77	P13: 84	P14: 87	P15: 87	P16: 93
P17: 68	P18: 67	P19: 69	P20: 69	P21: 78	P22: 90	P23: 85	P24: 88
P25: 65	P26: 66	P27: 69	P28: 67	P29: 74	P30: 88	P31: 85	P32: 84
P33: 65	P34: 65	P35: 67	P36: 66	P37: 74	P38: 85	P39: 84	P40: 82
P41: 67	P42: 66	P43: 72	P44: 72	P45: 78	P46: 89	P47: 79	P48: 80
P49: 73	P50: 70	P51: 71	P52: 80	P53: 89	P54: 83	P55: 76	P56: 76
P57: 90	P58: 85	P59: 83	P60: 82	P61: 92	P62: 87	P63: 88	P64: 78

Gain Map Normalized (Best Pixel = 100), from datasheet

Binary output imaged directly.
Use no ADC informations

Laser illuminated pixel,
1kHz, 405 nm, 2 attenuators, tune 30%
spe rate ~300 Hz

Preamp Gain Map used uncorrelated with datasheet (not optimized)

Conclusion

RICH Front End design almost complete

New methodologies for binary readout single channel analysis under development

Combination of HV and preamp gain investigation just started

Thanks to all the collegues for the fast, precise job and positive support!