RICH Electronics Update

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This week

1.Electronic schematics: .....slide 2
2.I/O requirements: Pin List ready .....slide 3,4
3.Boards Design: Proposal.....slide 5,6,7,8

ASIC board electronic scheme almost done.

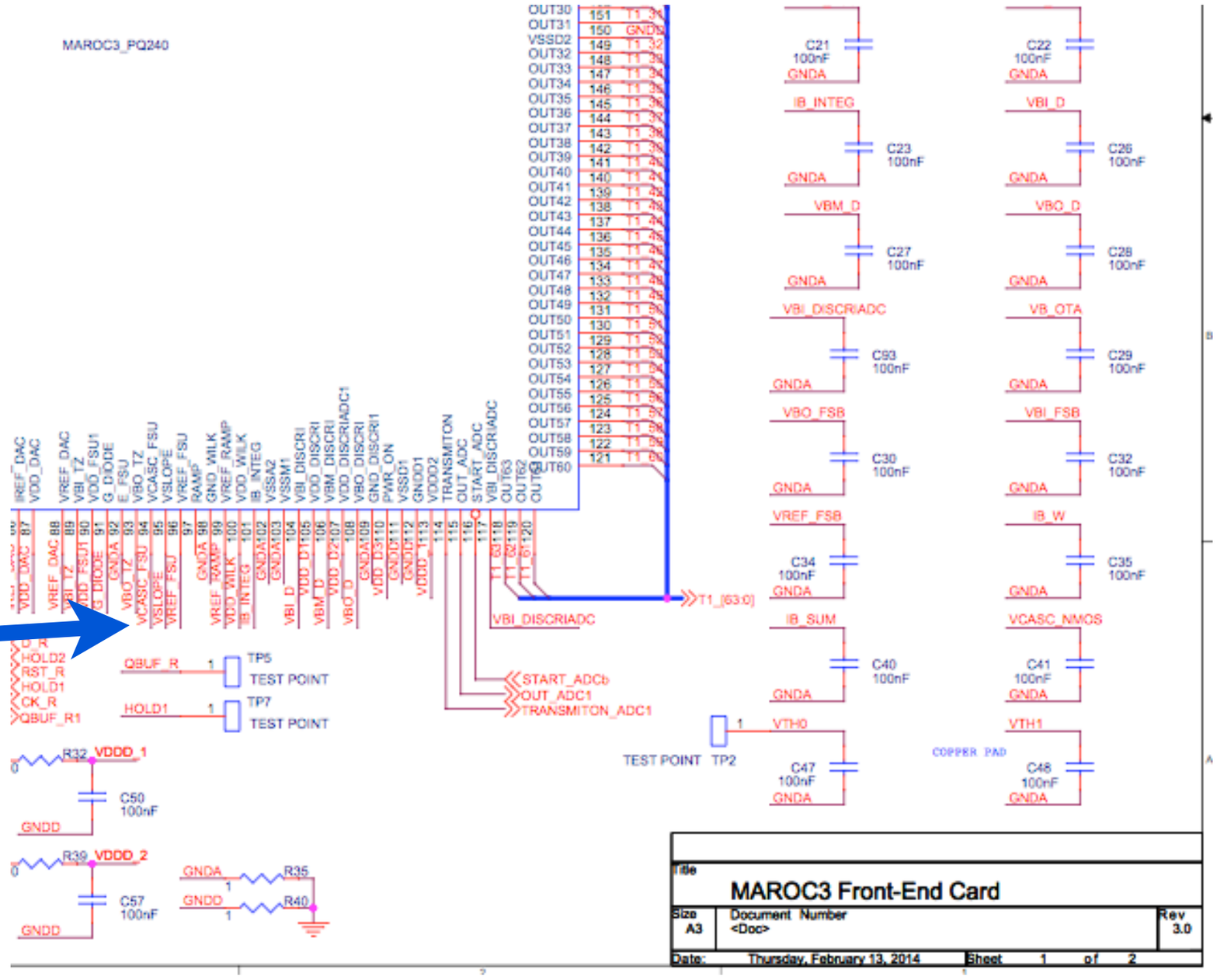
- 3 ASIC version.
- Updated ICs (tailored)

To Do:

- Check bias
- Set Test Points

Notes:

- One power line
- Less constraints than H8500 adapter board



I/O Connector Requirements

Spreadsheet for I/O pins calculation.
Easy maintainance.

1) Pin description

EXT ADC pin	EXT ADC name	I/O	LEVEL	FUNCTION	Top Level	multiplicity
	EN			ENABLE	EXTERNAL ADC	1
	CK			CLOCK	EXTERNAL ADC	1
	DOUT			DATA	EXTERNAL ADC	3

LV pin	Name		LEVEL	FUNCTION	Top Level	multiplicity
	VDD		4,0	POWER	LV	8
	GND		0	GND	LV	24

MAROC pin	MAROC name	I/O	LEVEL	FUNCTION	Top Level	multiplicity
79	Hold1	INPUT	TTL	EXT_TRIG	EXT_TRIG	1
81	Hold2	INPUT	TTL	EXT_TRIG	EXT_TRIG	1
76	Qbuf_R	OUTPUT	TTL	DYNAMIC REGISTER	MAROC	3
78	CK_R	INPUT	TTL	DYNAMIC REGISTER	MAROC	1
80	RSTb_R	INPUT	TTL	DYNAMIC REGISTER	MAROC	1
82	D_R	INPUT	TTL	DYNAMIC REGISTER	MAROC	3
64	D_SC	INPUT	TTL	STATIC REGISTER	MAROC	1
66	RSTn_SC	INPUT	TTL	STATIC REGISTER	MAROC	1
199	Qbuf_SC	OUTPUT	TTL	STATIC REGISTER	MAROC	1
68	CK_SC	INPUT	TTL	STATIC REGISTER	MAROC	1
114	TrasmitON	OUTPUT	HSTL	INTERNAL ADC	MAROC	3
115	OUT_ADC	OUTPUT	HSTL	INTERNAL ADC	MAROC	3
116	start_ADCb	INPUT	TTL	INTERNAL ADC	MAROC	1
186	CKb_40M	INPUT	LVDS	INTERNAL ADC	MAROC	1
188	CK_40M	INPUT	LVDS	INTERNAL ADC	MAROC	1
213	EN_otaq	INPUT	TTL	DONTKNOW	MAROC	1
234	Ctest	INPUT	ANALOG	TEST PULSE	TEST PULSE	1
191	OR_0	OUTPUT	TTL	MASKED OR	MAROC	3
192	OR_1	OUTPUT	TTL	MASKED OR	MAROC	3
118	out<63>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3
119	out<62>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3
120	out<61>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3
121	out<60>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3
122	out<59>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3
123	out<58>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3
124	out<57>	OUTPUT	HSTL	TRIGGER BIT	MAROC	3

Gran total on next slide...

2) Number of ASIC on board as parameter

# asic	note
3	equal to the number of external ADC

3) Summary MAROC

	Total [# pins]	
TRIGGER BIT	192	Binary Output (parallel)
MASKED OR	6	Binary Output (OR)
DYNAMIC REGISTER	8	Charge Multiplexer
STATIC REGISTER	4	Configuration
INTERNAL ADC	9	Charge Digital output
DONTKNOW	1	Enable OTA
TOTAL	220	

TOP LEVEL

	Total [# pins]
MAROC	220
LV	32
EXT_TRIG	2
EXTERNAL ADC	5
TEST PULSE	1
TOTAL	260

4) Many pins for the power line

5) Smart Solutions (Daisy Chain, Parallelism)

- External Trigger
- **MAROC3 Outputs**
- **Test signal** (fixed charge)
- **Read Register** (multiplex. charge)
- **Slow Control** (daisy chained)
- **Internal ADC**
- **External ADC**
- **Power Line** (regulators onboard)

Signals subgroup exchanged between ASIC and FPGA

ASIC-FPGA: Total Pin Number

TOP LEVEL

TOTAL			
MAROC	80	150	220
LV	32	32	32
EXT_TRIG	2	2	2
EXT_ADC	3	4	5
TEST PULSE	1	1	1
TOTAL	118	189	260

ASIC board 2 ASIC board 3

MAROC

	Total [# pins]	Total [# pins]	Total [# pins]	
TRIGGER BIT	64	128	192	Binary Output (parallel)
MASKED OR	2	4	6	Binary Output (OR)
DYNAMIC REGISTER	4	6	8	Charge Multiplexer
STATIC REGISTER	4	4	4	Configuration
INTERNAL ADC	5	7	9	Charge Digital output
DONTKNOW	1	1	1	Enable OTA
TOTAL	80	150	220	

Conclusions:

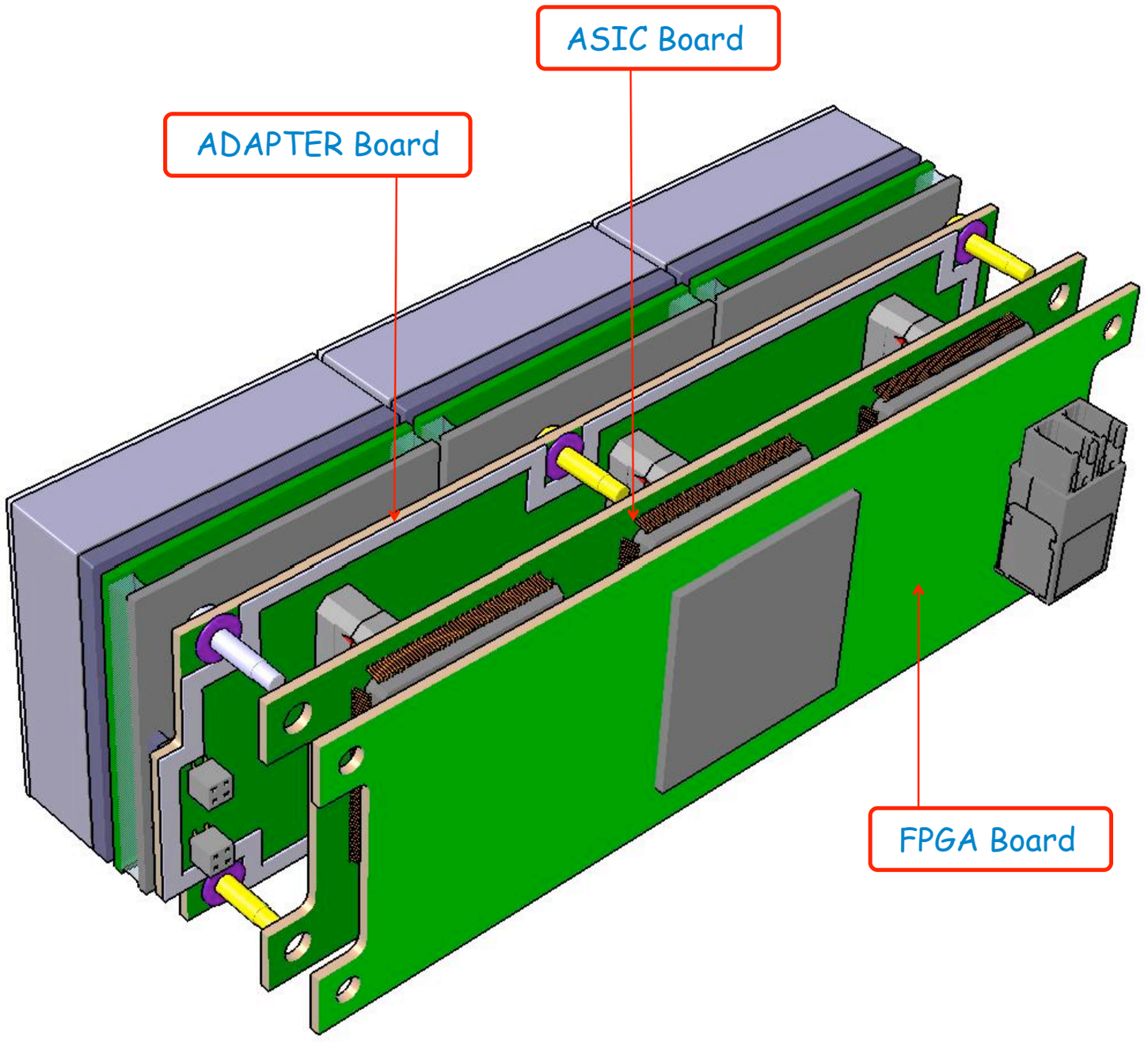
I/O requirements defined (easy maintenable)

Ready to assign pin name (set connector model before)

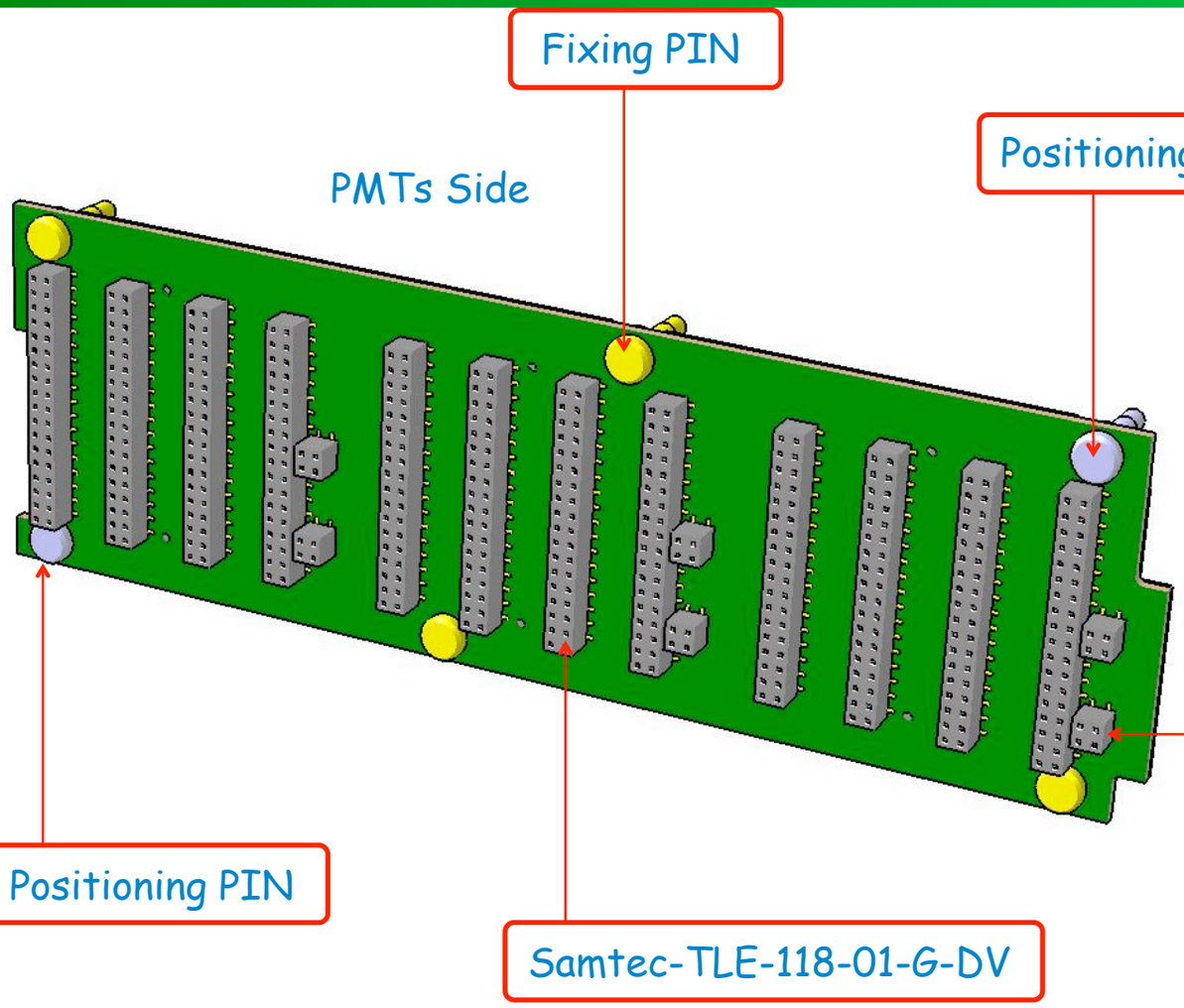
Proposal on the next slides

3 MAPMTs Tile

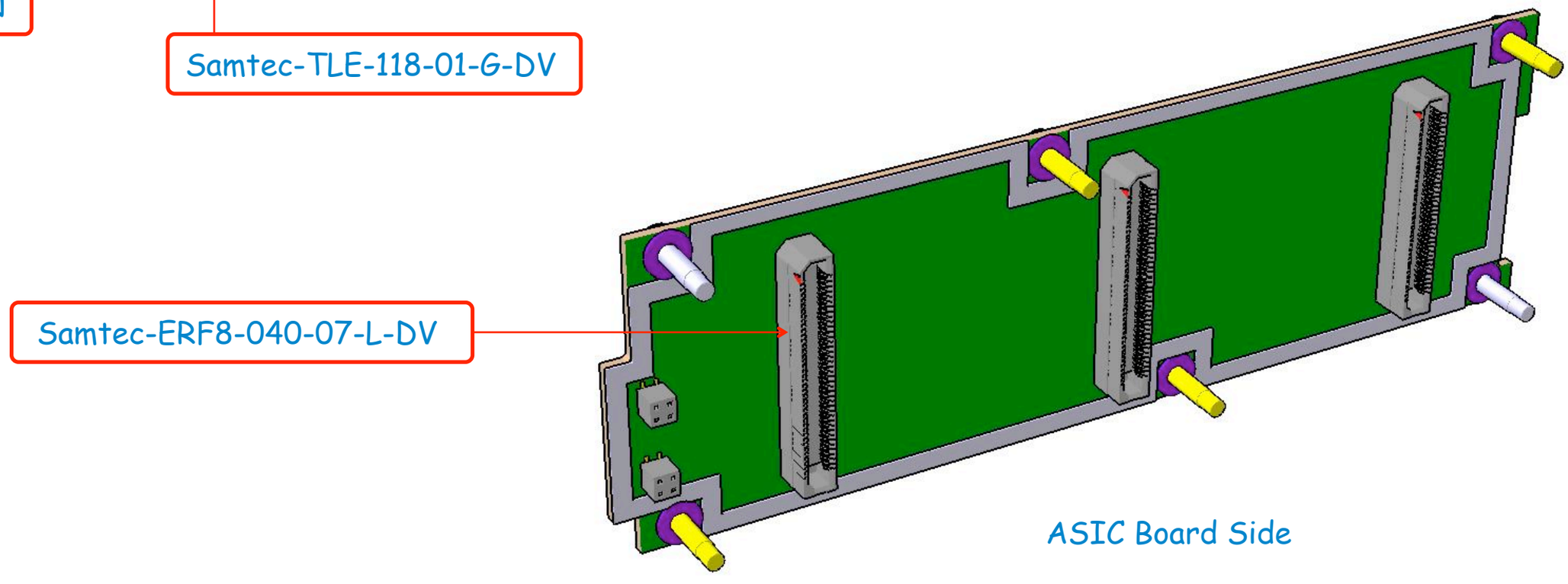
Ready to join electronics and mechanics developments together



H8500 Adapter Board

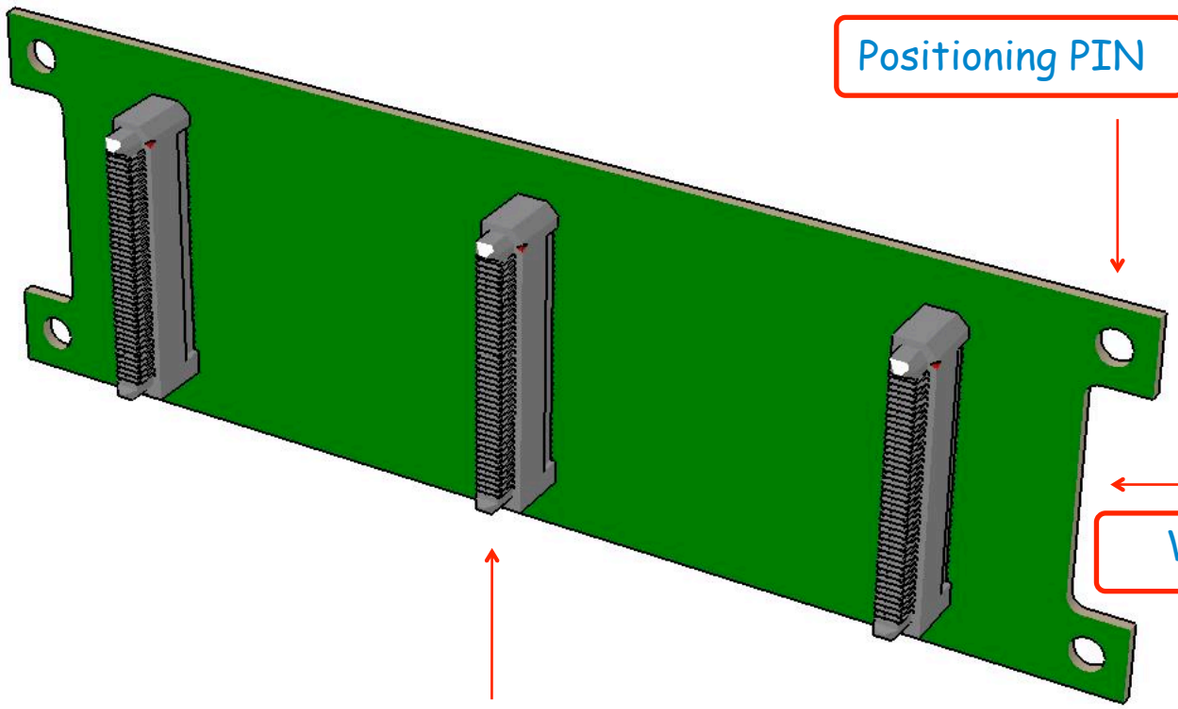


Must be light and gas tight!



ASIC Board

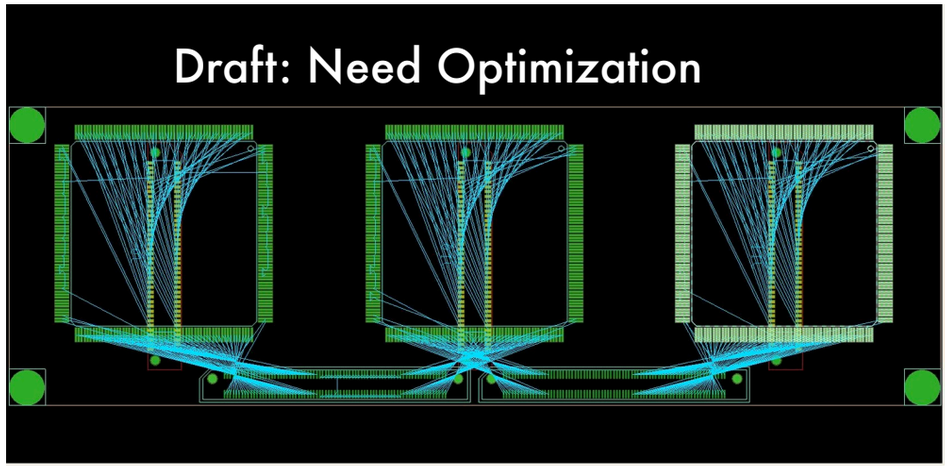
ADAPTER Side



Positioning PIN

Windows for air circulation

Samtec-ERM8-040-09.0-L-DV



Anodes paths, do they need to be equalized in length?

No, spread negligeable (50 ps/cm).

HSTL Voltage regulator on board

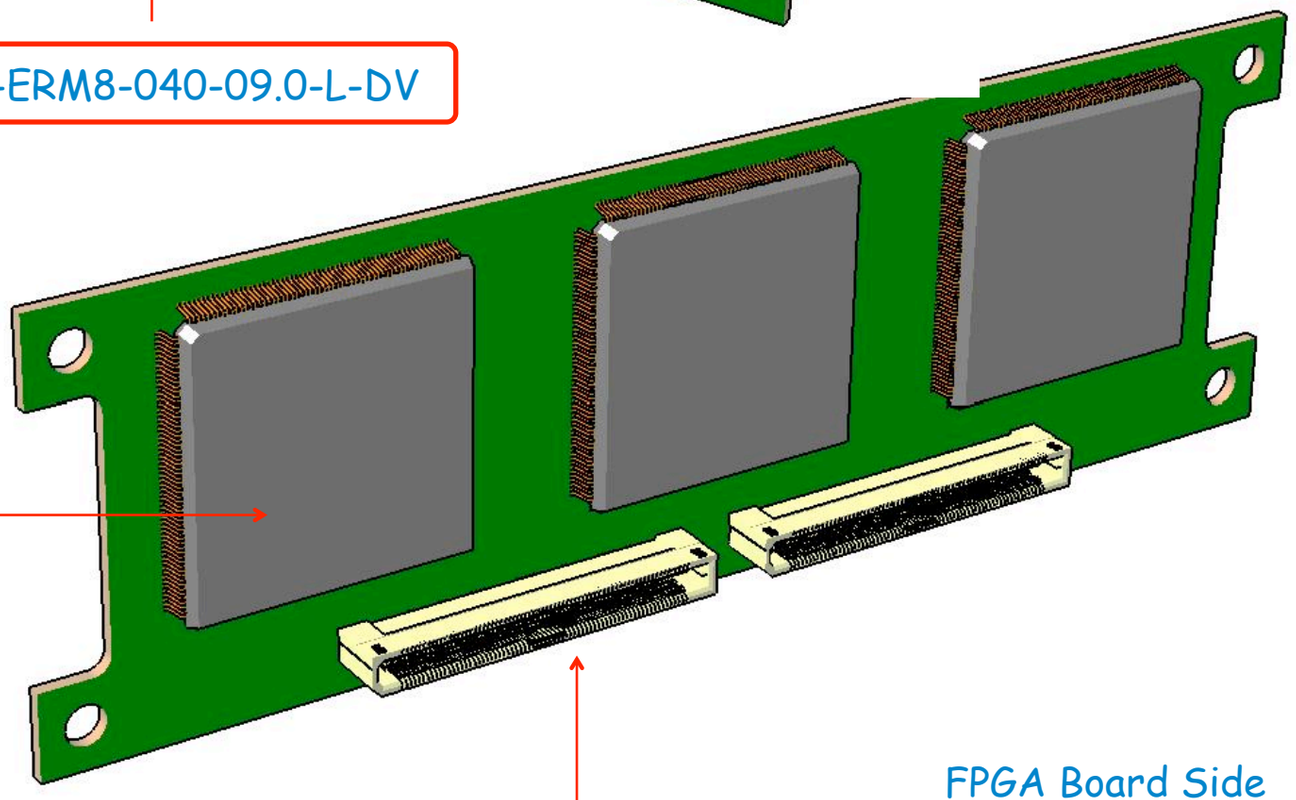
VH = 1.5 Volts

VL = 0.0 Volts

External ADC Voltage reference

V_ADC_REF = 3.0 Volts

MAROC



FPGA Board Side

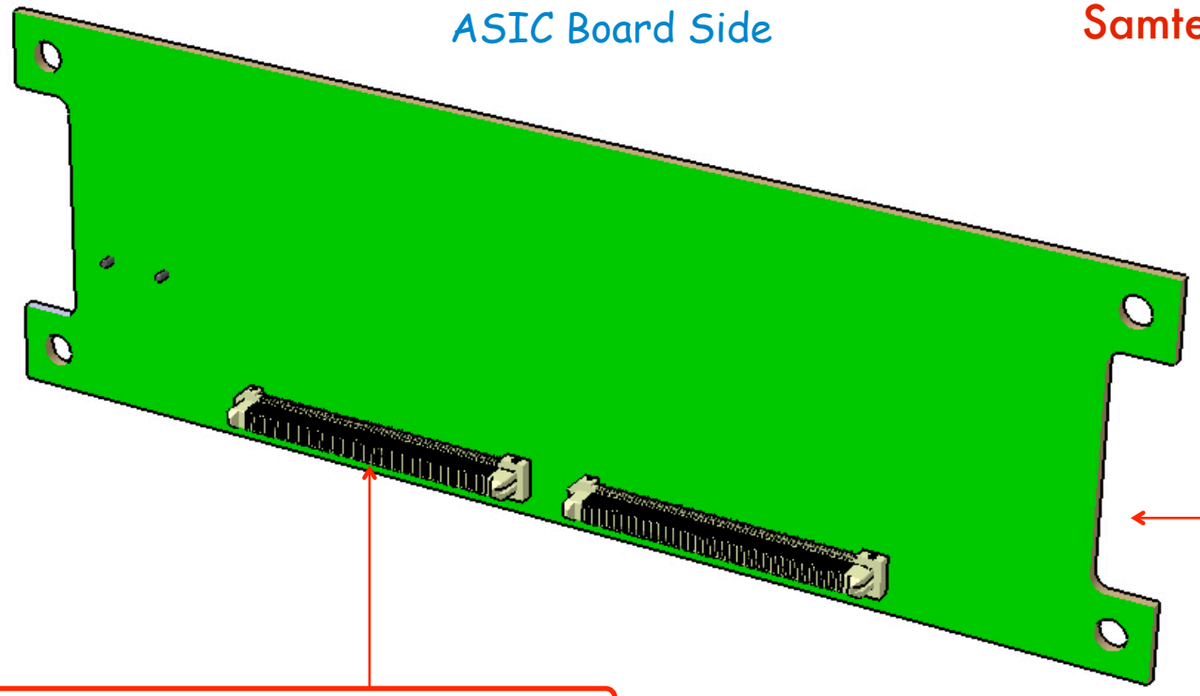
Samtec- ERF5-070-07.0-X-DV-K

Samtec Series 5 (70 pin per raws) implementation

FPGA Board

ASIC Board Side

Samtec Series 5 (70 pin per raws) implementation



Windows for air circulation

Samtec- ERM5-070-02.0-X-DV

Could we use just one kind of FPGA board?

Could it be 100 mm x 50 mm to facilitate the airflow?