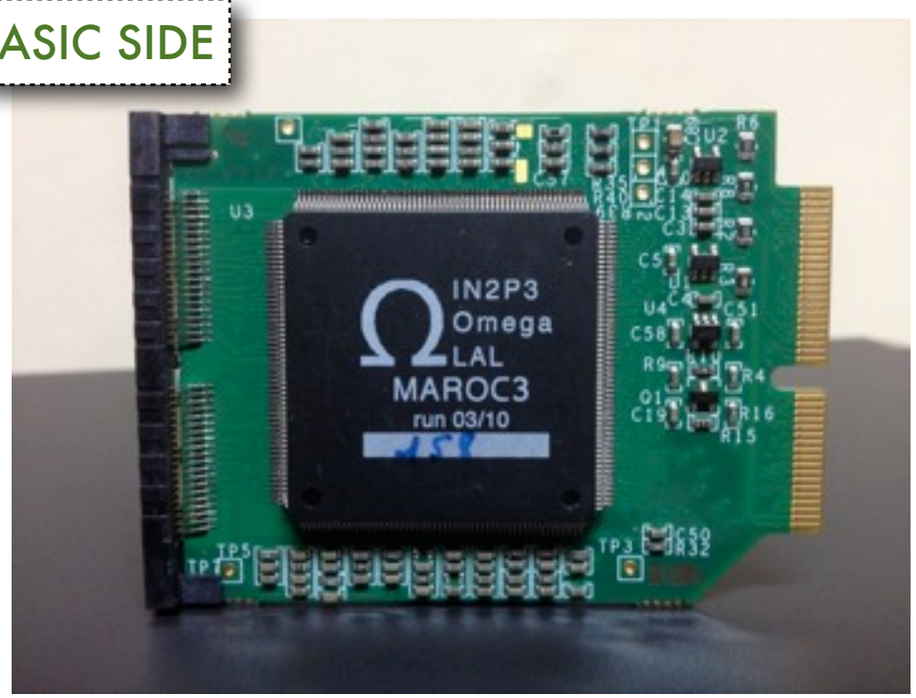
on ASIC Board

M.Turisini

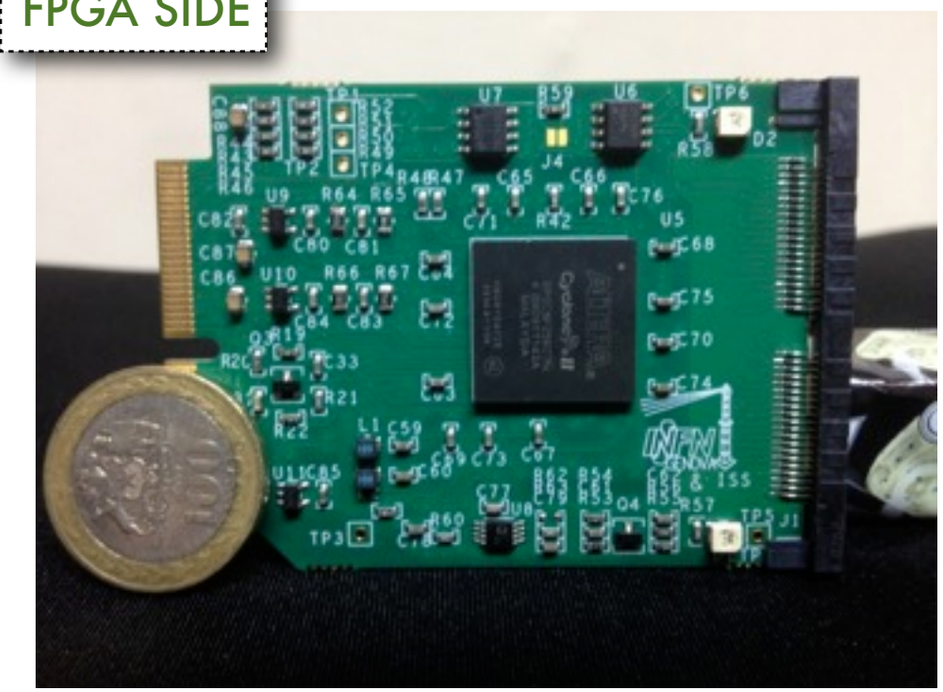
CLAS12 RICH Meeting, 2014 January 31th

Approach

ASIC SIDE



FPGA SIDE



- Start from current implementation revising and updating with more recent IC.
- Find smart and robust solution for 2 or 3 ASIC.
- Design for RICH having in mind bench tests.
- Some blocks could be placed on ASIC board or FPGA board with repercussions on available space on board and connectors pinout.

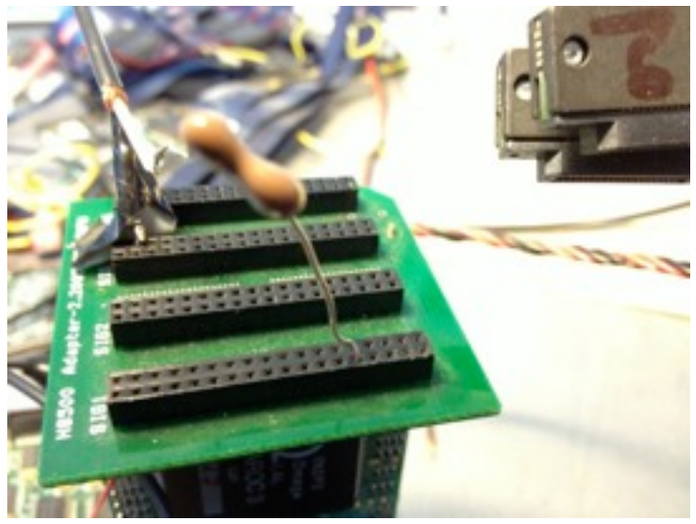
Interface with H8500,Test Pulses

- Anodes signal routing will be determined optimizing paths disentagle
- Current design join HV GND and LV GND at Support board level (large ground planes)

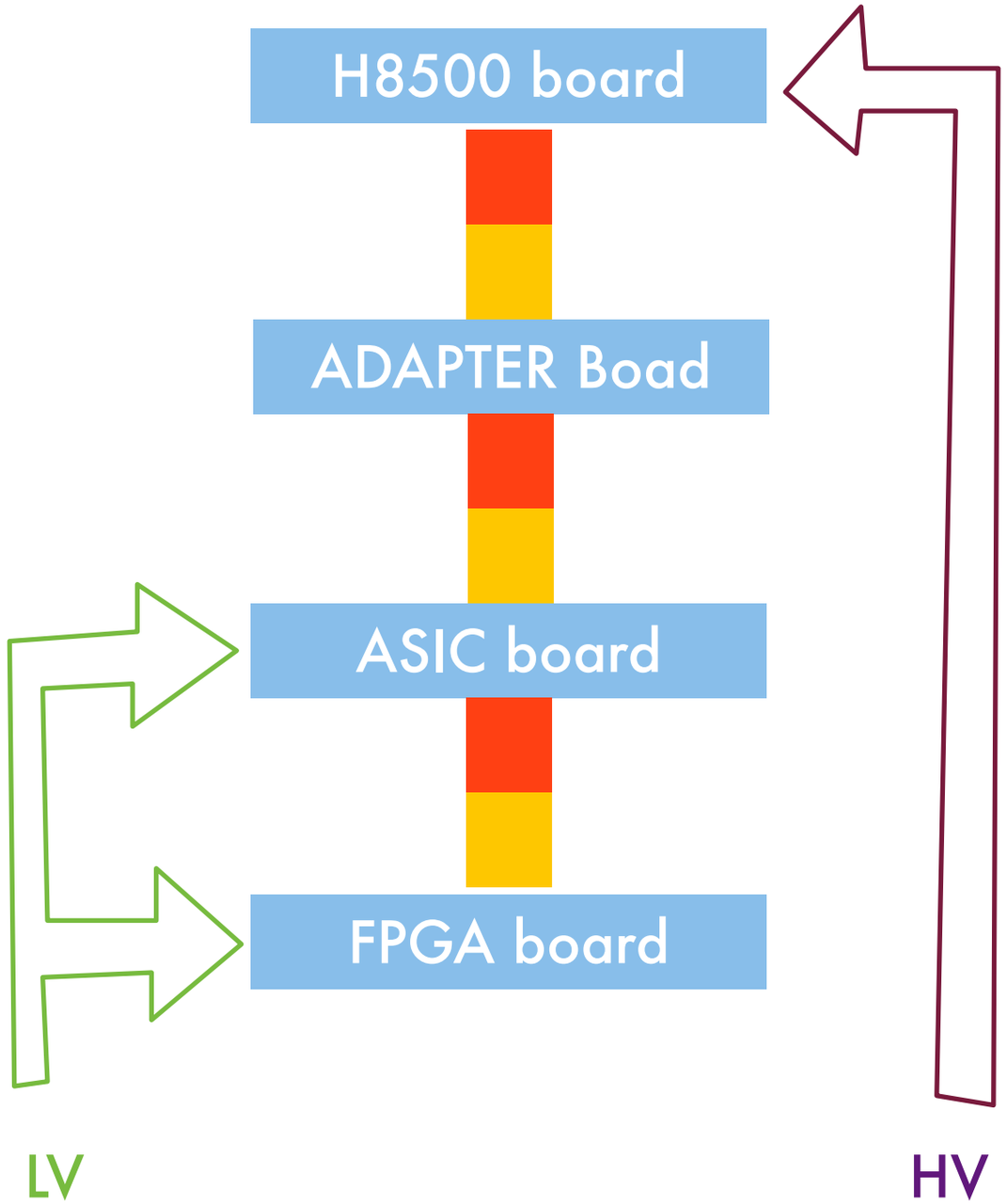
1) Who provide reference for anodes?

- Test pulse Enabled from FPGA, redesign charge injection circuit with newer IC.
- Actually on bench we never use dedicated circuitry, we just inject current in one anode channel on MAPMT Support board (current name is “H8500 Adaper Board”)

2) Do we need charge injector in CLAS?



Power Supply



- One power line (4 Volt) reaches the ASIC board where Analog Voltage reference (3.5Volt) and Digital Voltage Reference (3.3 Volt) are generated by voltage regulators. We will use most recent IC with greater maximum current, around 400mA max (for 3 ASIC supply)

3) Dedicated connector and cables or using pins and ground of the board-to-board connector?

4) HSTL voltage swing generated on FPGA board?

HV reaches H8500 board thanks to a cutout on both ASIC Board and FPGA Board. CAEN A1535N provides adequate power/ channel for the three MAPMT.

Connection with FPGA board

note: tables are for single asic

	MAROC PIN [#]
ADAPTER	64
TEST PULSE	1
FPGA	82
EXTERNAL ADC	1
POWER	21
GND	28
BIAS	30
NOT USED	13
TOTAL	240

	MAROC PIN [#]
STATIC REGISTER	4
DYNAMIC REGISTER	5
TRIGGER BIT	64
MASKED OR	2
INTERNAL ADC	7
EXTERNAL ADC	0
TOTAL	82

- 3 Parallel external ADC controlled by FPGA. Need extra pins on the connector. Detailed after ADC choice.

- FPGA configures and controls 2 or 3 ASICS
- Static register data will be daisy chained with paralleled CLK and RST
- Charge measurement needs a Delay Line (DL). If HOLD pins can share the same line is better to put the DL on FPGA board (saving the pins otherwise used for configuring DL and for routing HOLD signals)

Self Trigger is a key feature for calibrating the detector!
In that case the trigger comes from MAROC...