MAROC3 pinout
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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
1	in<3>	INPUT	ANALOG	ANODE	ADAPTER
2	in<4>	INPUT	ANALOG	ANODE	ADAPTER
3	in<5>	INPUT	ANALOG	ANODE	ADAPTER
4	in<6>	INPUT	ANALOG	ANODE	ADAPTER
5	in<7>	INPUT	ANALOG	ANODE	ADAPTER
6	in<8>	INPUT	ANALOG	ANODE	ADAPTER
7	in<9>	INPUT	ANALOG	ANODE	ADAPTER
8	in<10>	INPUT	ANALOG	ANODE	ADAPTER
9	in<11>	INPUT	ANALOG	ANODE	ADAPTER
10	in<12>	INPUT	ANALOG	ANODE	ADAPTER
11	in<13>	INPUT	ANALOG	ANODE	ADAPTER
12	in<14>	INPUT	ANALOG	ANODE	ADAPTER
13	in<15>	INPUT	ANALOG	ANODE	ADAPTER
14	in<16>	INPUT	ANALOG	ANODE	ADAPTER
15	in<17>	INPUT	ANALOG	ANODE	ADAPTER
16	in<18>	INPUT	ANALOG	ANODE	ADAPTER
17	in<19>	INPUT	ANALOG	ANODE	ADAPTER
18	in<20>	INPUT	ANALOG	ANODE	ADAPTER
19	in<21>	INPUT	ANALOG	ANODE	ADAPTER
20	in<22>	INPUT	ANALOG	ANODE	ADAPTER
21	in<23>	INPUT	ANALOG	ANODE	ADAPTER
22	in<24>	INPUT	ANALOG	ANODE	ADAPTER
23	in<25>	INPUT	ANALOG	ANODE	ADAPTER
24	in<26>	INPUT	ANALOG	ANODE	ADAPTER
25	in<27>	INPUT	ANALOG	ANODE	ADAPTER
26	in<28>	INPUT	ANALOG	ANODE	ADAPTER
27	in<29>	INPUT	ANALOG	ANODE	ADAPTER
28	in<30>	INPUT	ANALOG	ANODE	ADAPTER
29	in<31>	INPUT	ANALOG	ANODE	ADAPTER
30	gnd_pa	GND	DC	PREAMPLIFIER	GND
31	in<32>	INPUT	ANALOG	ANODE	ADAPTER
32	in<33>	INPUT	ANALOG	ANODE	ADAPTER
33	in<34>	INPUT	ANALOG	ANODE	ADAPTER
34	in<35>	INPUT	ANALOG	ANODE	ADAPTER
35	in<36>	INPUT	ANALOG	ANODE	ADAPTER

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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
36	in<37>	INPUT	ANALOG	ANODE	ADAPTER
37	in<38>	INPUT	ANALOG	ANODE	ADAPTER
38	in<39>	INPUT	ANALOG	ANODE	ADAPTER
39	in<40>	INPUT	ANALOG	ANODE	ADAPTER
40	in<41>	INPUT	ANALOG	ANODE	ADAPTER
41	in<42>	INPUT	ANALOG	ANODE	ADAPTER
42	in<43>	INPUT	ANALOG	ANODE	ADAPTER
43	in<44>	INPUT	ANALOG	ANODE	ADAPTER
44	in<45>	INPUT	ANALOG	ANODE	ADAPTER
45	in<46>	INPUT	ANALOG	ANODE	ADAPTER
46	in<47>	INPUT	ANALOG	ANODE	ADAPTER
47	in<48>	INPUT	ANALOG	ANODE	ADAPTER
48	in<49>	INPUT	ANALOG	ANODE	ADAPTER
49	in<50>	INPUT	ANALOG	ANODE	ADAPTER
50	in<51>	INPUT	ANALOG	ANODE	ADAPTER
51	in<52>	INPUT	ANALOG	ANODE	ADAPTER
52	in<53>	INPUT	ANALOG	ANODE	ADAPTER
53	in<54>	INPUT	ANALOG	ANODE	ADAPTER
54	in<55>	INPUT	ANALOG	ANODE	ADAPTER
55	in<56>	INPUT	ANALOG	ANODE	ADAPTER
56	in<57>	INPUT	ANALOG	ANODE	ADAPTER
57	in<58>	INPUT	ANALOG	ANODE	ADAPTER
58	in<59>	INPUT	ANALOG	ANODE	ADAPTER
59	in<60>	INPUT	ANALOG	ANODE	ADAPTER
60	in<61>	INPUT	ANALOG	ANODE	ADAPTER
61	IN<62>	INPUT	ANALOG	ANODE	ADAPTER
62	IN<63>	INPUT	ANALOG	ANODE	ADAPTER
63	gnd_pa	GND	DC	PREAMPLIFIER	GND
64	D_SC	INPUT	TTL	STATIC REGISTER	FPGA
65	vssa	GND	DC	?	GND
66	RSTn_SC	INPUT	TTL	STATIC REGISTER	FPGA
67	vdd_pa	AVDD	DC	PREAMPLIFIER	POWER
68	CK_SC	INPUT	TTL	STATIC REGISTER	FPGA
69	vgain_pa			PREAMPLIFIER	BIAS
70	ibi_ss			SLOW SHAPER	BIAS

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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
71	vcasc_pmos				BIAS
72	ibo_ss			SLOW SHAPER	BIAS
73	gnd_nmos	GND	DC	NMOS MIRROR	GND
74	ibi_buf				BIAS
75	vref_ss			SLOW SHAPER	BIAS
76	Qbuf_R	OUTPUT	TTL	INTERNAL ADC	FPGA
77	gnd_w	GND		WILKINSON ADC	GND
78	CK_R	INPUT	TTL	DYNAMIC REGISTER	FPGA
79	Hold1	INPUT	TTL	DYNAMIC REGISTER	FPGA
80	RSTb_R	INPUT	TTL	DYNAMIC REGISTER	FPGA
81	Hold2	INPUT	TTL	DYNAMIC REGISTER	FPGA
82	D_R	INPUT	TTL	DYNAMIC REGISTER	FPGA
83	vdd_w	POWER	DC		POWER
84	ibo_dac			DAC	BIAS
85	gnd_dac	GND	DC	DAC	GND
86	iref_dac			DAC	POWER
87	vdd_dac	POWER	DC	DAC	POWER
88	vref_dac			DAC	BIAS
89	vbi_tz			FSU1	BIAS
90	vdd_fsu1	POWER	DC	FSU1	POWER
91	G_diode			FSU1	BIAS
92	E_fsu	GND	DC	FSU1	GND
93	vbo_tz			FSU1	BIAS
94	vcasc_fsu			FSU1	BIAS
95	vslope	OUTPUT	Analog	WILKINSON ADC	BIAS
96	vref_fsu			FSU1	BIAS
97	ramp	OUTPUT	Analog	WILKINSON ADC	NOT USED
98	gnd_wilk	GND	DC	WILKINSON ADC	GND
99	vref_ramp	INPUT	Analog	WILKINSON ADC	BIAS
100	vdd_wilk	POWER	DC	WILKINSON ADC	POWER
101	ib_integ			WILKINSON ADC	BIAS
102	vssa	GND	DC		GND
103	vssm	GND	DC		GND
104	vbi_discri				BIAS

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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
105	vdd_discri	POWER	DC		POWER
106	vbm_discri				BIAS
107	vdd_discriADC	AVDD	DC		POWER
108	vbo_discri				BIAS
109	gnd_discri	GND	DC		GND
110	PWR_ON	AVDD	DC		POWER
111	vssd	GND	DC		GND
112	gnd	GND	DC		GND
113	vddd2	VDDD	DC		POWER
114	TrasmitON	OUTPUT	HSTL	INTERNAL ADC	FPGA
115	OUT_ADC	OUTPUT	HSTL	INTERNAL ADC	FPGA
116	start_ADCb	INPUT	TTL	INTERNAL ADC	FPGA
117	vbi_discriADC				BIAS
118	out<63>	OUTPUT	HSTL	TRIGGER BIT	FPGA
119	out<62>	OUTPUT	HSTL	TRIGGER BIT	FPGA
120	out<61>	OUTPUT	HSTL	TRIGGER BIT	FPGA
121	out<60>	OUTPUT	HSTL	TRIGGER BIT	FPGA
122	out<59>	OUTPUT	HSTL	TRIGGER BIT	FPGA
123	out<58>	OUTPUT	HSTL	TRIGGER BIT	FPGA
124	out<57>	OUTPUT	HSTL	TRIGGER BIT	FPGA
125	out<56>	OUTPUT	HSTL	TRIGGER BIT	FPGA
126	out<55>	OUTPUT	HSTL	TRIGGER BIT	FPGA
127	out<54>	OUTPUT	HSTL	TRIGGER BIT	FPGA
128	out<53>	OUTPUT	HSTL	TRIGGER BIT	FPGA
129	out<52>	OUTPUT	HSTL	TRIGGER BIT	FPGA
130	out<51>	OUTPUT	HSTL	TRIGGER BIT	FPGA
131	out<50>	OUTPUT	HSTL	TRIGGER BIT	FPGA
132	out<49>	OUTPUT	HSTL	TRIGGER BIT	FPGA
133	out<48>	OUTPUT	HSTL	TRIGGER BIT	FPGA
134	out<47>	OUTPUT	HSTL	TRIGGER BIT	FPGA
135	out<46>	OUTPUT	HSTL	TRIGGER BIT	FPGA
136	out<45>	OUTPUT	HSTL	TRIGGER BIT	FPGA
137	out<44>	OUTPUT	HSTL	TRIGGER BIT	FPGA
138	out<43>	OUTPUT	HSTL	TRIGGER BIT	FPGA
139	out<42>	OUTPUT	HSTL	TRIGGER BIT	FPGA

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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
140	out<41>	OUTPUT	HSTL	TRIGGER BIT	FPGA
141	out<40>	OUTPUT	HSTL	TRIGGER BIT	FPGA
142	out<39>	OUTPUT	HSTL	TRIGGER BIT	FPGA
143	out<38>	OUTPUT	HSTL	TRIGGER BIT	FPGA
144	out<37>	OUTPUT	HSTL	TRIGGER BIT	FPGA
145	out<36>	OUTPUT	HSTL	TRIGGER BIT	FPGA
146	out<35>	OUTPUT	HSTL	TRIGGER BIT	FPGA
147	out<34>	OUTPUT	HSTL	TRIGGER BIT	FPGA
148	out<33>	OUTPUT	HSTL	TRIGGER BIT	FPGA
149	out<32>	OUTPUT	HSTL	TRIGGER BIT	FPGA
150	vssd	GND	DC		GND
151	out<31>	OUTPUT	HSTL	TRIGGER BIT	FPGA
152	out<30>	OUTPUT	HSTL	TRIGGER BIT	FPGA
153	out<29>	OUTPUT	HSTL	TRIGGER BIT	FPGA
154	out<28>	OUTPUT	HSTL	TRIGGER BIT	FPGA
155	out<27>	OUTPUT	HSTL	TRIGGER BIT	FPGA
156	out<26>	OUTPUT	HSTL	TRIGGER BIT	FPGA
157	out<25>	OUTPUT	HSTL	TRIGGER BIT	FPGA
158	out<24>	OUTPUT	HSTL	TRIGGER BIT	FPGA
159	out<23>	OUTPUT	HSTL	TRIGGER BIT	FPGA
160	out<22>	OUTPUT	HSTL	TRIGGER BIT	FPGA
161	out<21>	OUTPUT	HSTL	TRIGGER BIT	FPGA
162	out<20>	OUTPUT	HSTL	TRIGGER BIT	FPGA
163	out<19>	OUTPUT	HSTL	TRIGGER BIT	FPGA
164	out<18>	OUTPUT	HSTL	TRIGGER BIT	FPGA
165	out<17>	OUTPUT	HSTL	TRIGGER BIT	FPGA
166	out<16>	OUTPUT	HSTL	TRIGGER BIT	FPGA
167	out<15>	OUTPUT	HSTL	TRIGGER BIT	FPGA
168	out<14>	OUTPUT	HSTL	TRIGGER BIT	FPGA
169	out<13>	OUTPUT	HSTL	TRIGGER BIT	FPGA
170	out<12>	OUTPUT	HSTL	TRIGGER BIT	FPGA
171	out<11>	OUTPUT	HSTL	TRIGGER BIT	FPGA
172	out<10>	OUTPUT	HSTL	TRIGGER BIT	FPGA
173	out<9>	OUTPUT	HSTL	TRIGGER BIT	FPGA
174	out<8>	OUTPUT	HSTL	TRIGGER BIT	FPGA

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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
175	out<7>	OUTPUT	HSTL	TRIGGER BIT	FPGA
176	out<6>	OUTPUT	HSTL	TRIGGER BIT	FPGA
177	out<5>	OUTPUT	HSTL	TRIGGER BIT	FPGA
178	out<4>	OUTPUT	HSTL	TRIGGER BIT	FPGA
179	out<3>	OUTPUT	HSTL	TRIGGER BIT	FPGA
180	out<2>	OUTPUT	HSTL	TRIGGER BIT	FPGA
181	out<1>	OUTPUT	HSTL	TRIGGER BIT	FPGA
182	out<0>	OUTPUT	HSTL	TRIGGER BIT	FPGA
183	gnd	GND	DC	DC	GND
184	RSTn_ADC	INPUT	TTL	INTERNAL ADC	FPGA
185	vddd	VDDD	DC	DC	POWER
186	CKb_40M	INPUT	LVDS	INTERNAL ADC	FPGA
187	VL	INPUT	ANALOG	HSTL “Low	POWER
188	CK_40M	INPUT	LVDS	INTERNAL ADC	FPGA
189	vssd	GND			GND
190	VH	INPUT	ANALOG	HSTL “high”	POWER
191	OR_0	OUTPUT	TTL	MASKED OR	FPGA
192	OR_1	OUTPUT	TTL	MASKED OR	FPGA
193	vdd_discriADC	POWER		WILKINSON ADC	POWER
194	vth1	OUTPUT	DC	DAC0 MONITOR	NOT USED
195	gnd_discri	GND		WILKINSON ADC	GND
196	vth0	OUTPUT	DC	DAC1 MONITOR	NOT USED
197	vssm	GND			GND
198	vss	GND			GND
199	Qbuf_SC	OUTPUT	DIGITAL	STATIC REGISTER	NOT USED
200	v_bg	OUTPUT	ANALOG		BIAS
201	out_fs	OUTPUT	ANALOG	OUTPUT FS	NOT USED
202	gnd_fsu	GND	DC	FSU	GND
203	vb_otafsu			FSU	BIAS
204	vdd_fsu2	POWER		FSU2	POWER
205	vbo_fsb			FSB1	BIAS
206	gnd_fsb1	GND	DC	FSB1	GND
207	vbi_fsb			FSB1	BIAS
208	vref_fsb			FSB1	BIAS

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Pin	name	I/O	SIGNAL	SUB-CIRCUIT	I/OConnection
209	ib_w				BIAS
210	vdd_fsb	AVDD	DC	FSB	POWER
211	gnd_fsb0	GND	DC	FSB	GND
212	ib_sum			SUM	BIAS
213	EN_otaq	INPUT	TTL	should be 3.3 Volt	FPGA
214	sum8	OUTPUT	ANALOG	SUM[56..63]	NOT USED
215	out_q	OUTPUT	ANALOG	Charge Output	EXTERNAL ADC
216	sum7	OUTPUT	ANALOG	SUM[48..55]	NOT USED
217	gnd_capa	GND	DC		GND
218	sum6	OUTPUT	ANALOG	SUM[40..47]	NOT USED
219	gnd_ss	GND	DC		GND
220	sum5	OUTPUT	ANALOG	SUM[32..39]	NOT USED
221	vdd_ss	AVDD	DC		POWER
222	sum4	OUTPUT	ANALOG	SUM[24..31]	NOT USED
223	vdd_buf1	AVDD	DC		POWER
224	sum3	OUTPUT	ANALOG	SUM[16..23]	NOT USED
225	vdd_otaq	AVDD	DC		POWER
226	sum2	OUTPUT	ANALOG	SUM [8..15]	NOT USED
227	gnd_otaq	GND	DC		GND
228	sum1	OUTPUT	ANALOG	SUM [0..7]	NOT USED
229	vcasc_nmos			NMOS MIRROR	BIAS
230	vbi_pa			PREAMPLIFIER	BIAS
231	gnd_nmos	GND	DC	NMOS MIRROR	GND
232	NC				BIAS
233	vdd_pa	AVDD	DC	PREAMPLIFIER	POWER
234	Ctest	INPUT	ANALOG	TEST PULSE	TEST PULSE
235	vssi	GND	DC		GND
236	vdd_pad	AVDD	DC	NMOS MIRROR	POWER
237	gnd_pa	GND	DC	PREAMPLIFIER	GND
238	in<0>	INPUT	ANALOG	ANODE	ADAPTER
239	in<1>	INPUT	ANALOG	ANODE	ADAPTER
240	in<2>	INPUT	ANALOG	ANODE	ADAPTER