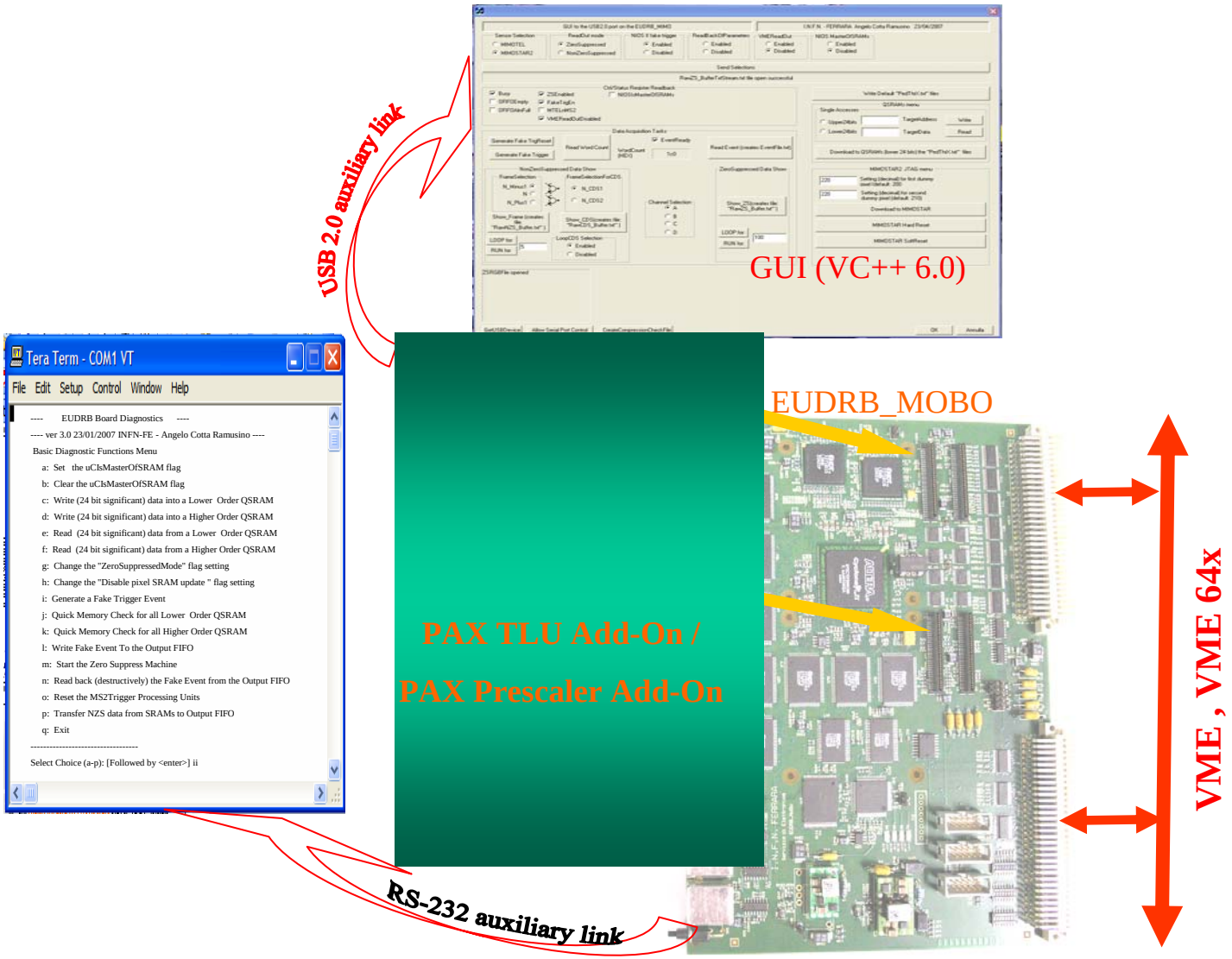


PAX Add-On Modules: PAX Trigger Logic Unit and PreScaler Unit as add-on card for the EUDET readout board (VME 64x based DAQ card)

STATUS REPORT

INFN Istituto Nazionale di Fisica Nucleare

Introduction:

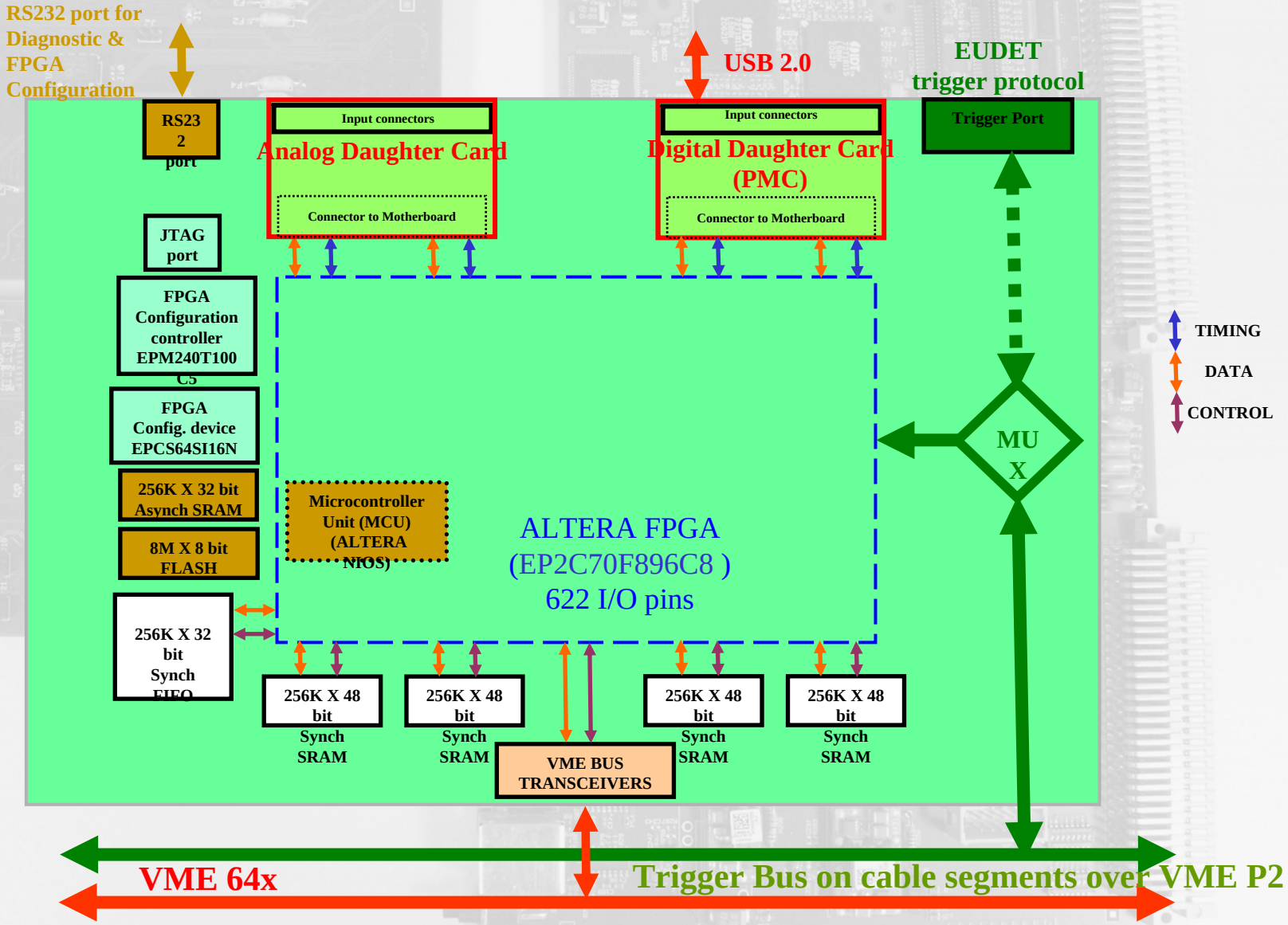
The EUDRB_MOBO (EUDET Readout Board, MotherBoard) is based on an ALTERA Cyclone II FPGA with an on-board NIOS-II microprocessor with 1MB external RAM. The board has 8MB of data memory (256K*4*48bits) and an output FIFO 32bit wide and 256K deep.

The EUDRB_MOBO has a VME 64x interface and it has also a serial and a USB2.0 link for stand-alone operation.

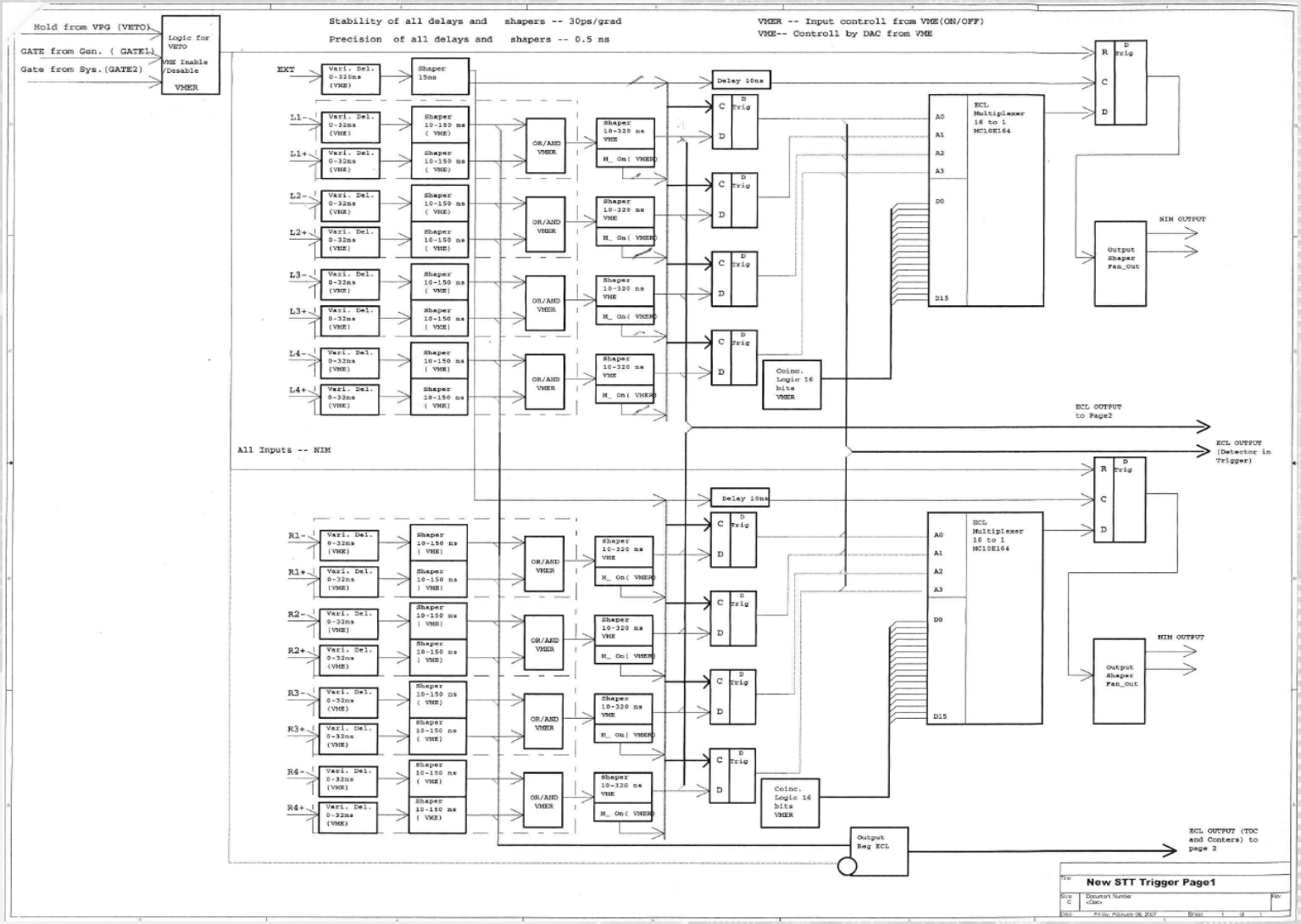
My proposal is to use one EUDRB_MOBO as the carrier for the PAX Trigger Logic Unit and for the PAX Prescaler Unit.

New EUDRB_MOBOs (1 spare available now for PAX development) can be produced in about 8 weeks and cost about 1600Euros

Introduction: overview of the EUDRB card

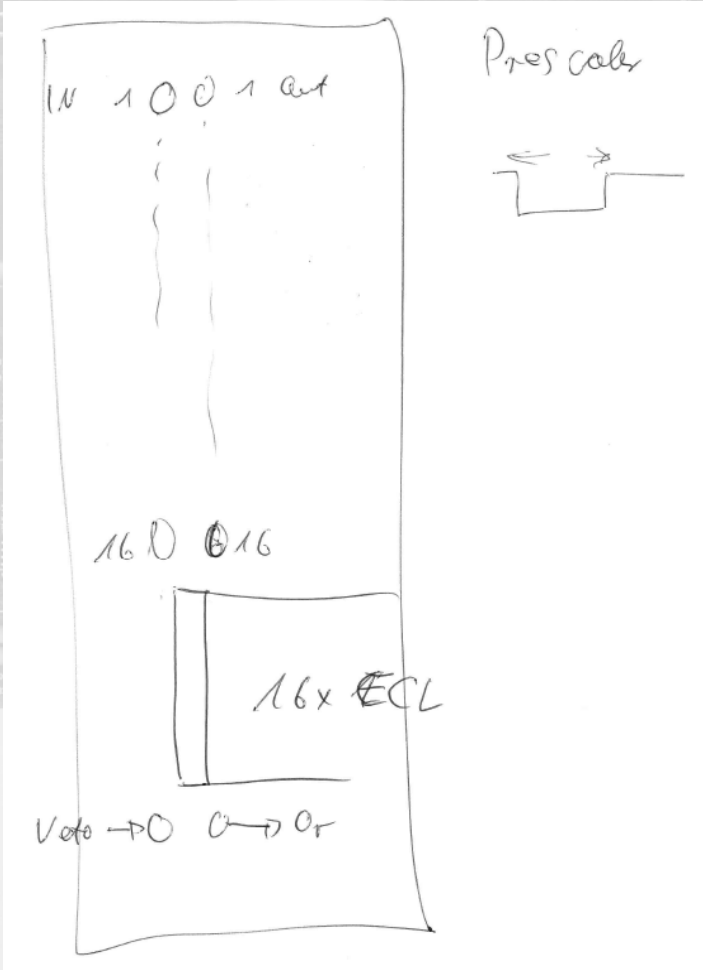


PAX Trigger Logic Unit specifications (Juelich FSZ)



TLU is specified to a full extent

PAX Prescaler Unit specifications (Juelich FSZ)



PreScaler still needing further specifications

PAX Trigger Logic Unit market search for components (A.C.R.)

PROJECT: TRIGGER SYSTEM FOR SILICON DETECTORS ("ANKE-PAX")
COMPONENT LIST for market survey
Angelo Cotta Ramusino, INFN-Ferrara, May 03 2007

							OFF-LINE			ARROW			AVNET/MEMEC				RS		DDD Europe		
TYPE	MANUFACTURER	PART NUMBER	PB-FREE	PACKAGE	parts per package	Supply voltages	LEAD TIME (wks.)	COST/100pcs	MOQ(pieces)	LEAD TIME (wks.)	COST/100pcs	MOQ(pieces)	LEAD TIME (wks.)	COST/100pcs	MOQ(pieces)	LEAD TIME (wks.)	COST/100pcs	MOQ(pieces)	LEAD TIME (wks.)	COST/10pcs	MOQ(pieces)
	ECL LEVEL TRANSLATORS																				
diff ECL to TTL	ONSEMI	MC10ELT25DG	YES	SOIC-8NB	1		stock	2,35	196	7	2,03	294									
diff ECL to TTL	ONSEMI	MC10ELT25DTG	YES	TSSOP-8	1					5	2,12	100									
TTL to diff ECL	ONSEMI	MC10ELT24DG	YES	SOIC-8NB	1		6	2,35	196	6	2,03	294									
TTL to diff ECL	ONSEMI	MC10ELT24DTG	YES	TSSOP-8	1					5	2,12	100									
Quad TTL to MECL translator	ONSEMI	MC10H124MG	YES	SOEIAJ-16	4		10	3,6	200	11	3,38	50									
Quad MECL to TTL translator	ONSEMI	MC10H125MG	YES	SOEIAJ-16	4					11	3,38	50									
Triple "Anylevel" to NECL	ONSEMI	MC100EP91DWG	YES	SO-20	3					8	10,3	76									
Dual "Anylevel" to LVDS	ONSEMI	NB4N527SMNG	YES	QFN-16	2	3.3V	6	5,75	246	4	5,45	123									
	PECL LEVEL TRANSLATORS																				
diff PECL to TTL	ONSEMI	MC100ELT23DG	YES	SOIC-8NB	2		stock	2,35	196	stock	2,1	98				stock	7,42	1			
TTL to (diff)PECL	ONSEMI	MC100ELT20DG	YES	SOIC-8NB	1											stock	7,2	1			
	COMPARATORS WITH ECL OUTPUTS																				
	Analog Devices	ADCMP572BCPZ								3	9,5	50									
Comparator diff ECL output	Analog Devices	ADCMP566BCP		LFCSP-32	2	5V, -5.2V	10/06/2007	3,9	200												
Comparator diff ECL output	MAXIM	MAX9691EUA		8uMAX	1	5V, -5.2V	10/06/2007	4,1	100												
Comparator diff ECL output	MAXIM	MAX9691ESA		8SO	1	5V, -5.2V	10/06/2007	2,95	100												
	COMPARATORS WITH PECL OUTPUTS																				
Comparator diff 5VpECL output	MAXIM	MAX9601EUP		20TSSOP	2	5V, -5.2V	10	5,95	222												
Comparator diff 3.3 pECL output	Analog Devices	ADCMP567BCP		LFCSP-32	2	5V, -5.2V, 3.3V	10/06/2007	3,99	200	3	3,6	50									
Comparator diff 3.3 pECL output	Analog Devices	ADCMP562BRQ		QSOP-20	2	5V, -5.2V, 3.3V	10/06/2007	3,99	200	3	3,6	50				stock	7,55	1			
	5V ECL LOGIC																				
5V ECL AND NAND, 2 IN S.E.	ONSEMI	MC100EL04DG	YES	SOIC-8NB	1		6	3,2	196	6	2,7	196									
5V ECL AND NAND, 2 IN S.E.	ONSEMI	MC100EL04DTG	YES	TSSOP-8	1					5	2,8	100									
5V ECL OR NOR 4 IN S.E.	ONSEMI	MC100EL01DG	YES	SOIC-8NB	1		6	3,2	196	6	2,7	196									
5V ECL OR NOR 4 IN S.E.	ONSEMI	MC100EL01DTG	YES	TSSOP-8	1					5	2,85	100									
5V ECL 2:1 MUX S.E.	ONSEMI	MC100EL58DG	YES	SOIC-8NB	1		stock	3,8	196	6	3,3	196									
5V ECL 2:1 MUX S.E.	ONSEMI	MC100EL58DTG	YES	TSSOP-8	1					5	3,4	100									
5V ECL 16:1 MUX S.E.	ONSEMI	MC100E164FNG	YES	PLCC-28	1		6	6,9	111	6	6,3	74									
5V ECL D-FF w/SET,RESET	ONSEMI	MC100EL31DG	YES	SOIC-8NB	1		stock	3,45	196	6	3	196									
5V ECL D-FF w/SET,RESET	ONSEMI	MC100EL31DTG	YES	TSSOP-8	1					5	3,1	100									
	DELAY LINES																				
8BIT PROGRAMMABLE SILICON DELAY LINE	MAXIM DALLAS	DS1023S-25	YES	SOIC 16	1	5V	6	8,75	135				15/06/2007	8,2	45						
8BIT PROGRAMMABLE SILICON DELAY LINE	MAXIM DALLAS	DS1023S-100	YES	SOIC 16	1	5V	10	9,2	135												
8BIT PROGRAMMABLE SILICON DELAY LINE	MAXIM DALLAS	DS1020S-25	YES	SOIC 16	1	5V										prenotazione	9,64	1			
4BIT PROGRAMMABLE ECL DELAY MODULES	www.rhombus-ind.com	PPECL2-5			1	-5.2V															
3BIT PROGRAMMABLE ECL DELAY MODULES	www.rhombus-ind.com	PECL3-5			1	-5.2V															
8bit Programmable Pulse Generator (0.5ns step)	Data Delay Devices, inc.	3D7608R-0.5		SOIC 16	1	5V	2	21,5	100										1	23,52	10
12bit Programmable Pulse Generator (0.25ns step)	Data Delay Devices, inc.	3D7612V-0.25		SOL 20	1	5V	2	16,8	100										1	28,22	10
QUAD 4BIT PROGRAMMABLE SILICON DELAY LINE (5ns step)	Data Delay Devices, inc.	3D7424-5		SOIC 14	4	5V	2	7,5	400										1	10,36	10
QUAD 4BIT PROGRAMMABLE SILICON DELAY LINE (5ns step)	Data Delay Devices, inc.	3D7424-2		SOIC 14	4	5V	2	7,5	400										1	10,36	10
QUAD 4BIT PROGRAMMABLE SILICON DELAY LINE (5ns step)	Data Delay Devices, inc.	3D7424-1		SOIC 14	4	5V	2	7,5	400										1	10,36	10
	12bit quad DACs WITH BIPOLAR OUTPUTS																				
12bit quad DACs WITH BIPOLAR OUTPUTS	BURR BROWN	DAC7614U		SOIC 16	4	5V, -5.2V															

PAX Trigger Logic Unit market search for components (A.C.R.)

3D7608 & 3D7612

8-BIT & 12-BIT PROGRAMMABLE PULSE GENERATORS

(SERIES 3D7608 & 3D7612: PARALLEL INTERFACE)

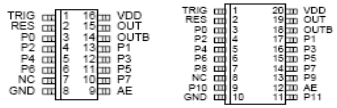
data delay devices, inc.

FEATURES

- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Programmable via latched parallel interface
- **Increment range:** 0.25ns through 800us
- **Pulse width tolerance:** 1% (See Table 1)
- **Supply current:** 8mA typical
- **Temperature stability:** ±1.5% max (-40C to 85C)
- **Vdd stability:** ±0.5% max (4.75V to 5.25V)

RoHS Compliant

PACKAGES / PINOUTS



3D7608R-xx SOIC 3D7612W-xx SOL

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7608 & 3D7612 devices are versatile 8- & 12-bit programmable monolithic pulse generators. A rising-edge on the trigger input (TRIG) initiates the pulse, which is presented on the output pins (OUT,OUTB). The pulse width, programmed via the parallel interface, can be varied over 255 (3D7608) or 4095 (3D7612) equal steps according to the formula:

$$t_{PW} = t_{inh} + addr * t_{inc}$$

where addr is the programmed address, t_{inc} is the pulse width increment (equal to the device dash number), and t_{inh} is the inherent (address zero) pulse width. The device also offers a reset input (RES), which can be used to terminate the pulse before the programmed time has expired.

The all-CMOS 3D7608 & 3D7612 integrated circuits have been designed as reliable, economic alternatives to hybrid TTL pulse generators. The 3D7608 is offered in a standard 16-pin SOIC, and the 3D7612 is offered in a standard 20-pin SOL.

PIN DESCRIPTIONS

TRIG	Trigger Input
RES	Reset Input
OUT	Pulse Output
OUTB	Complementary Pulse Output
AE	Address Enable Input
P0-P11	Address Inputs
VDD	+5 Volts
GND	Ground
NC	Do not connect externally

TABLE 1: PART NUMBER SPECIFICATIONS

PART # (8-BIT)	PART # (12-BIT)	Pulse Width Increment	Maximum P.W. (8-Bit)	Maximum P.W. (12-Bit)
3D7608R-0.25	3D7612W-0.25	0.25ns ± 0.12ns	73.25ns ± 3ns	1.03us ± 10ns
3D7608R-0.5	3D7612W-0.5	0.50ns ± 0.25ns	137.5ns ± 3ns	2.05us ± 21ns
3D7608R-1	3D7612W-1	1.0ns ± 0.5ns	265ns ± 3ns	4.10us ± 41ns
3D7608R-2	3D7612W-2	2.0ns ± 1.0ns	520ns ± 6ns	8.19us ± 82ns
3D7608R-5	3D7612W-5	5.0ns ± 2.5ns	1.28us ± 13ns	20.5us ± 205ns
3D7608R-10	3D7612W-10	10ns ± 5.0ns	2.56us ± 26ns	41.0us ± 410ns
3D7608R-20	3D7612W-20	20ns ± 10ns	5.11us ± 52ns	81.9us ± 819ns
3D7608R-50	3D7612W-50	50ns ± 25ns	12.8us ± 128ns	205us ± 2.1us
3D7608R-100	3D7612W-100	100ns ± 50ns	25.5us ± 255ns	410us ± 4.1us
3D7608R-200	3D7612W-200	200ns ± 100ns	51.0us ± 510ns	819us ± 8.2us
3D7608R-500	3D7612W-500	500ns ± 250ns	128us ± 1.3us	2.05ms ± 21us
3D7608R-1K	3D7612W-1K	1.0us ± 0.5us	255us ± 2.6us	4.10ms ± 41us
3D7608R-2K	3D7612W-2K	2.0us ± 1.0us	510us ± 5.2us	8.19ms ± 82us
3D7608R-5K	3D7612W-5K	5.0us ± 2.5us	1.28ms ± 13us	20.5ms ± 205us
3D7608R-10K	3D7612W-10K	10us ± 5us	2.56ms ± 26us	41.0ms ± 410us
3D7608R-20K	3D7612W-20K	20us ± 10us	5.11ms ± 52us	81.9ms ± 819us
3D7608R-50K	3D7612W-50K	50us ± 25us	12.8ms ± 128us	205ms ± 2.1 ms

PART # (8-BIT)	Pulse Width Increment	Maximum P.W. (8-Bit)
3D7608R-100K	100us ± 50us	25.5ms ± 260us
3D7608R-200K	200us ± 100us	51.0ms ± 510us
3D7608R-500K	500us ± 250us	128ms ± 1.3ms
3D7608R-800K	800us ± 400us	204ms ± 2.1ms

NOTE: Any increment between 0.25ns and 800us (50us for the 12-bit generator) not shown is also available as a standard device.

PULSEWIDTH STABILITY: 250ppm/C

~30 Euro each

3D7424

MONOLITHIC QUAD 4-BIT PROGRAMMABLE DELAY LINE (SERIES 3D7424)

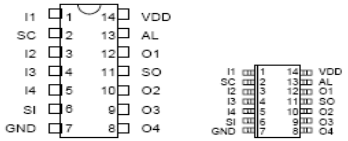
data delay devices, inc.

FEATURES

- Four indep't programmable lines on a single chip
- All-silicon CMOS technology
- Low quiescent current (5mA typical)
- Leading- and trailing-edge accuracy
- Vapor phase, IR and wave solderable
- **Increment range:** 0.75ns through 400ns
- **Delay tolerance:** 3% or 2ns (see Table 1)
- **Line-to-line matching:** 1% or 1ns typical
- **Temperature stability:** ±1.5% typical (-40C to 85C)
- **Vdd stability:** ±0.5% typical (4.75V to 5.25V)
- **Minimum input pulse width:** 10% of total delay

RoHS Compliant

PACKAGES



DIP-14 3D7424-xx SOIC-14 3D7424D-xx

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7424 device is a small, versatile, quad 4-bit programmable monolithic delay line. Delay values, programmed via the serial interface, can be independently varied over 15 equal steps. The step size (in ns) is determined by the device dash number. Each input is reproduced at the corresponding output without inversion, shifted in time as per user selection. For each line, the delay time is given by:

$$TD_n = T0 + A_n * TI$$

where T0 is the inherent delay, A_n is the delay address of the n-th line and TI is the delay increment (dash number). The desired addresses are shifted into the device via the SC and SI inputs, and the addresses are latched using the AL input. The serial interface can also be used to enable/disable each delay line. The 3D7424 operates at 5 volts and has a typical T0 of 6ns. The 3D7424 is TTL/CMOS-compatible, capable of sourcing or sinking 4mA loads, and features both rising- and falling-edge accuracy. The device is offered in a standard 14-pin auto-insertable DIP and a space saving surface mount 14-pin SOIC.

PIN DESCRIPTIONS

I1-I4	Signal Inputs
O1-O4	Signal Outputs
AL	Address Latch In
SC	Serial Clock In
SI	Serial Data In
SO	Serial Data Out
VDD	5.0V
GND	Ground

TABLE 1: PART NUMBER SPECIFICATIONS

Part Number	DELAYS & TOLERANCES (NS) Delay Step	Inherent Delay	Total Delay	Relative Tolerance	INPUT RESTRICTIONS Max Frequency Recom'd	Max Frequency Absolute	Min Pulse Width Recom'd	Min Pulse Width Absolute
3D7424-.75	.75 ± 0.19	6.0 ± 2.0	17.25 ± 2.0	3% or 0.50ns	19 MHz	166 MHz	26 ns	3.0 ns
3D7424-1	1.0 ± 0.25	6.0 ± 2.0	21.0 ± 2.0	3% or 0.50ns	16 MHz	166 MHz	32 ns	3.0 ns
3D7424-1.5	1.5 ± 0.38	6.0 ± 2.0	28.5 ± 2.0	3% or 0.50ns	12 MHz	111 MHz	43 ns	4.5 ns
3D7424-2	2.0 ± 0.50	6.0 ± 2.0	36.0 ± 2.0	3% or 0.75ns	9.2 MHz	83 MHz	54 ns	6.0 ns
3D7424-4	4.0 ± 1.00	6.0 ± 2.0	66.0 ± 2.0	3% or 0.75ns	5.0 MHz	83 MHz	99 ns	6.0 ns
3D7424-5	5.0 ± 1.25	6.0 ± 2.0	81.0 ± 2.5	3% or 0.75ns	4.1 MHz	66 MHz	122 ns	7.5 ns
3D7424-10	10 ± 2.50	6.0 ± 2.0	156 ± 5.0	3% or 1.25ns	2.1 MHz	33 MHz	234 ns	15.0 ns
3D7424-15	15 ± 3.75	6.0 ± 2.0	231 ± 7.5	3% or 1.88ns	1.4 MHz	22 MHz	347 ns	22.5 ns
3D7424-20	20 ± 5.00	6.0 ± 2.0	306 ± 10	3% or 2.50ns	1.0 MHz	16 MHz	459 ns	30.0 ns
3D7424-40	40 ± 10.0	6.0 ± 2.0	606 ± 20	3% or 5.00ns	550 KHz	8.3 MHz	909 ns	60.0 ns
3D7424-50	50 ± 10.0	6.0 ± 2.0	756 ± 25	3% or 6.25ns	440 KHz	6.6 MHz	1.2 us	75.0 ns
3D7424-100	100 ± 12.5	6.0 ± 2.0	1506 ± 50	3% or 12.5ns	220 KHz	3.3 MHz	2.3 us	150 ns
3D7424-200	200 ± 25.0	6.0 ± 2.0	3006 ± 100	3% or 25.0ns	110 KHz	1.7 MHz	4.5 us	300 ns
3D7424-400	400 ± 50.0	6.0 ± 2.0	6006 ± 200	3% or 50.0ns	55 KHz	830 KHz	9.0 us	600 ns

NOTE: Any increment between 0.75ns and 400ns not shown is also available as Standard.
See page 4 for details regarding input restrictions

DELAY STABILITY: 250ppm/C

~10 Euro each

Samples of key components have been received

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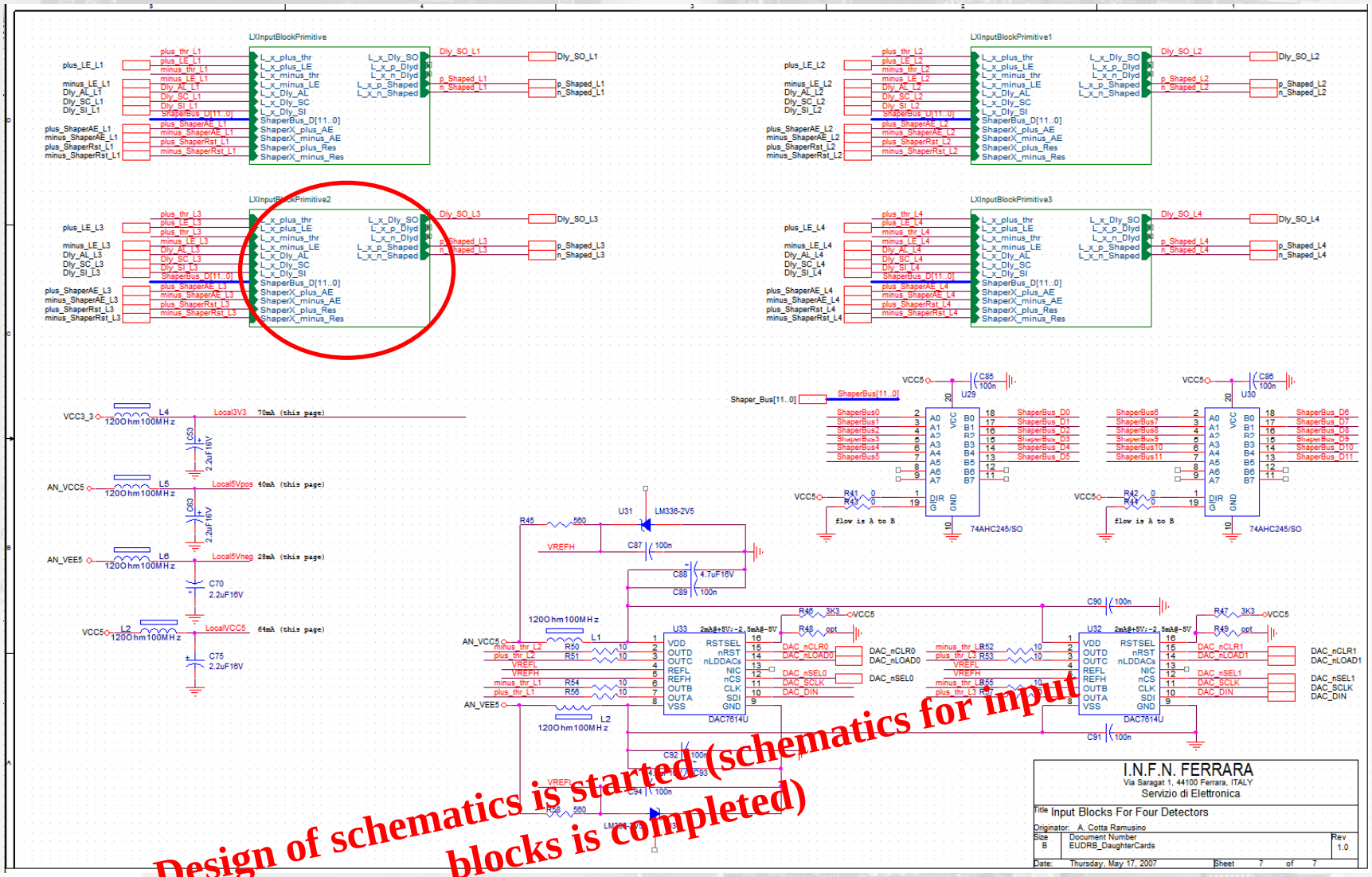
PAX Trigger Logic Unit schematics (A.C.R.)



Design of schematics is started (schematics for input blocks is completed)

PAX Trigger Logic Unit schematics (A.C.R.)